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Application Note: AS3933-AN04 – Design Guide

AS3933

AN04 – Design Guide

Table of Contents

Revision History

Revision	Date	Owner	Description
1.0	16.07.2013	JRY	Initial Release

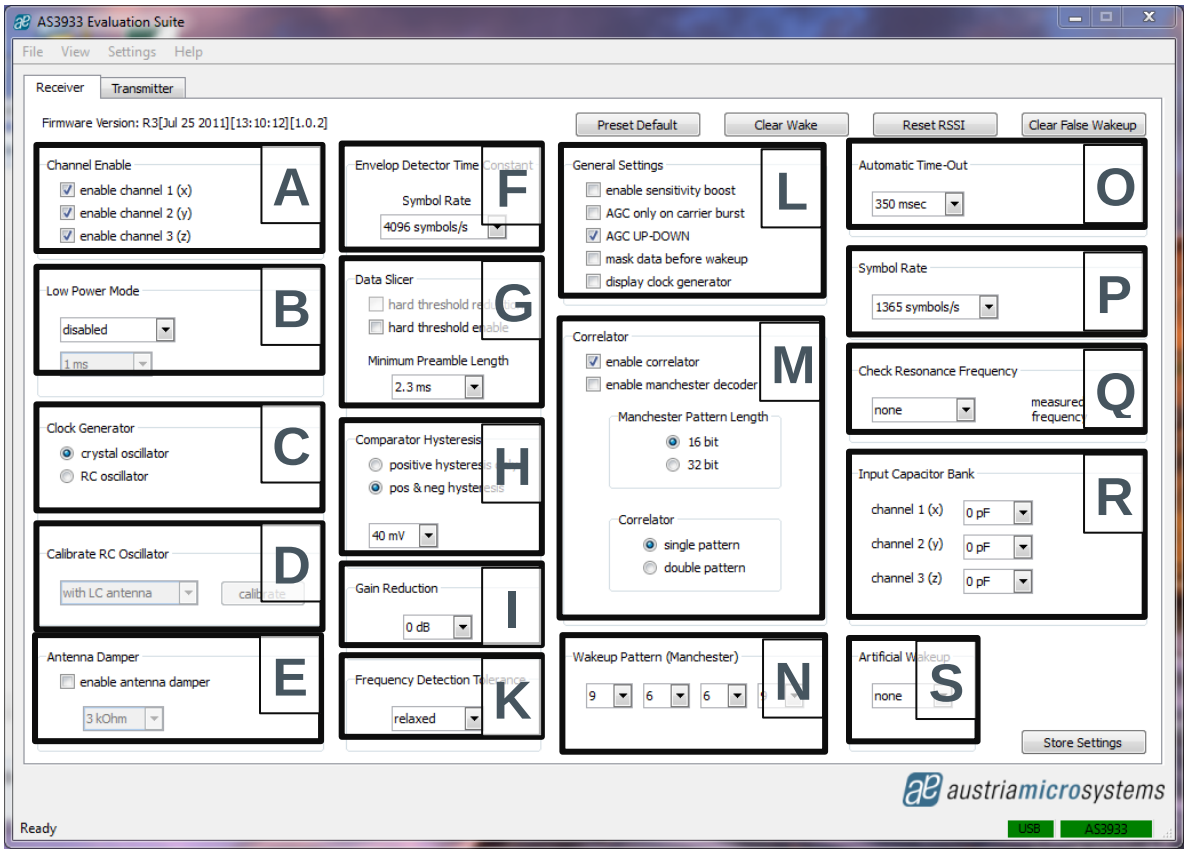
1 General Description

This application note is intended to guide the design-in of the AS3933. An examples will be used to show how to set the register map in order to achieve the desired performance. Furthermore, some aspects that need to be considered when designing the hardware and choosing components will be mentioned.

2 Link of GUI settings to datasheet

In this section it will explained which registers are affected when changing settings in the GUI and where the respective descriptions can be found in the datasheet. The datasheet referred to is revision 1.4.

Figure 1: Link between GUI settings and datasheet.



Pos.	Description	Register	Datasheet	Table
A	Enable/disable channel	R0<3:1>	Section 8.1.1, 8.3, 8.10	8
B	Enable/disable low power modes	R0<5:4>, R4<7:6>	Section 8.1.1, 8.10	8
C	Choose clock generator	R1<0>, R2<6>	Section 8.8	8, 26, 27, 29
D	Calibrate RC oscillator	R1<0>, R14<7:0>	Section 8.8.2	28

Pos.	Description	Register	Datasheet	Table
E	Enable/disable antenna damper	R1<4>, R4<5:4>	Section 8.3.2	8, 19
F	Envelope detector time constant	R3<2:0>	Section 8.4	8, 20
G	Data slicer settings	R1<7>, R2<7>, R3<5:3>,	Section 8.4	8, 21
H	Data slicer hysteresis settings	R3<7:6>	Section 8.4	8
I	Gain reduction settings	R4<3:0>	Section 8.3	8, 18
K	Frequency detector tolerance	R2<1:0>	Section 8.3.1	8, 16, 17
L	Sensitivity boost	R2<5>	Section 8.3.1	8
	AGC settings	R1<6:5>	Section 8.3.1	8
	Mask data	R0<6>	Section 8.1.3	8
	Display clock generator	R2<3:2>, R16<7>	Section 8.8	8
M	Correlator settings	R0<7>, R1<3:1>	Section 8.1.3, 8.5, 8.6, 8.7	8
N	Wakeup pattern	R5<7:0>, R6<7:0>	Section 8.5, 8.6	8
O	Automatic time-out settings	R7<7:5>	Section 8.3	8, 23
P	Bit rate settings	R7<4:0>	Section 8.5	8, 22
Q	Measure resonance frequency of each antenna tank	R1<4>, R4<5:4>, R16<2:0>	Section 8.9	8
R	Internal parallel capacitance for antenna tuning	R17<4:0>, R18<4:0>, R19<4:0>	Section 8.9	8, 30, 31, 32
S	Artificial Wakeup settings	R8<2:0>	Section 8.1.2	8

3 AS3933 – Design example

3.1 AS3933 settings

3.1.1 Carrier frequency

The first parameter that should be defined is the carrier frequency f_{carr}. In case the frequency can be chosen randomly the question would be what the surrounding looks like. If there are other devices operating in a certain band, it might make sense to choose a different one for the AS3933 to minimize the noise. Let us choose f_{carr} = 125 kHz for this example. Thus, we need to set bits R8<7:5> = 000 to select the frequency range that includes f_{carr} as shown in Figure 2 (table 15 DS).

Figure 2: Carrier frequency

R8<7>	R8<6>	R8<5>	N	Operating Frequency Range [kHz]
0	0	0	4	95-150
0	0	1	6	65-95
0	1	0	10	40-65
0	1	1	18	23-40
1	1	1	14	15-23

With this information the required clock generator period can be calculated. In Figure 3 (table 26 in the datasheet) the relation $f_{RC} = f_{carr}/4$ is given, which yields f_{RC} = 31.25 kHz ($T_{clk} = 1/f_{RC}$ = 32 µs). This leads us to the next design decision: what should be the source of f_{RC}?

Figure 3: Clock generator frequency

Carrier Frequency [kHz]	Clock Generator Frequency
15 – 23	$f_{RC} = f_{carr} \cdot \frac{14}{8}$
23 – 40	$f_{RC} = f_{carr} \cdot \frac{9}{8}$
40-65	$f_{RC} = f_{carr} \cdot \frac{5}{8}$
65 – 95	$f_{RC} = f_{carr} \cdot \frac{3}{8}$
95 - 150	$f_{RC} = \frac{f_{carr}}{4}$

3.1.2 Clock Source

The AS3933 gives us three choices: external quartz, the internal RC oscillator, or providing the clock from an external source such as a microcontroller. There are advantages and disadvantages to these options. On the one hand, the external quartz increases the BOM by three components (quartz + two load capacitors) and depending on the frequency the quartz can get rather expensive. On the other hand it will yield a very accurate time base. The RC oscillator does not need extra space or components, but needs to be calibrated. That requires an accurate reference clock somewhere in the system and the calibration must be implemented in the firmware. In case an

accurate external source with the necessary clock frequency is available, the external source would be the simplest solution. However, if components such as a microcontroller need to be powered during inactive periods only to provide the clock to the wakeup receiver, this choice would increase the power consumption.

With these thoughts in mind let us choose a quartz oscillator. Epson has a crystal in its portfolio with the correct frequency: C-2 31.2500K-P. In the register map the crystal oscillator needs to be enabled: R1<0> =1.

3.1.3 Frequency detection tolerance

We can now choose the tight frequency detection tolerance to already make the system less sensitive towards noise. This is done by setting R2<1:0> = 10. How the frequency detection works is described in section 8.3.1 of the datasheet. Table 15 gives us the length of one time window; $4xT_{clk}$ = 128 µs in this particular case. In Figure 4 (table 16 DS) the detection tolerance is given for the used band. For the chosen tolerance the frequency detector must measure 16 ± 2 zero crossings in two consecutive time windows. This means that the frequency must be in the range of $\frac{14}{128\ \mu s} < f < \frac{18}{128\ \mu s}$. The AS3933 will only start the wakeup procedure in case the measured frequency is within a range of 109.375 kHz < f <140.625 kHz.

Figure 4: Tolerance for frequency detection – bands 23 - 150 kHz

R2<1>	R2<0>	M
0	0	16±6
0	1	16±4
1	0	16±2
1	1	n.a.

3.1.4 Low Power Mode

There are three possible operation modes which we can choose from: standard listening mode, On/Off mode, and scanning mode. The On/Off mode and scanning mode are low power listening modes. The On/Off mode works by only listening for a 1ms time interval and then shutting off for a definable time. The scanning mode works by listening on one channel at a time. The standard listening mode, however, has all the selected channels enabled all the time. Let us use the scanning mode to save power → R0<4> = 1.

3.1.5 Channel selection

The AS3933 features three channels. Therefore, the signal can be detected in all three dimensions. Let us assume that the system can only receive the signal from two directions. We can disable one channel to save power. The channel that needs to be deactivated in this case is channel 2 as described in section 8.10 → R0<3> = 0.

3.1.6 Carrier Burst

With the carrier frequency and the operation mode defined, the minimum duration of the carrier burst can be calculated. As we use the scanning mode we need to consult Figure 5 (table 25 of the datasheet). For our operating frequency range we have the definition: $T_{burst} \geq 80xT_{clk} + 16xT_{carr} =$

2.688 ms. Furthermore, it needs to be shorter than 155xT_{clk} = 4.96 ms as described in section 8.6.2 of the datasheet. Let us choose 3 ms for simplicity.

Figure 5: Minimum duration of the carrier burst – scanning mode enabled

Operating Frequency Range [kHz]	Minimum Duration of the Carrier Burst
95-150	80·Tclk+16Tcarr
65-95	92·Tclk+16Tcarr
40-65	180·Tclk+16Tcarr
23-40	224Tclk+16Tcarr
15-23	220·Tclk+8Tcarr

3.1.7 Bit rate

Let us assume that the bit rate is not yet defined by the system. We then have the choice between the maximum of 7.812 kb/s down to the minimum 0.976 kb/s. These settings are defined in table 22 of the datasheet and need to be set in register R7<4:0>. Choosing a higher bit rate will require more bandwidth from the antenna and make the system more sensitive towards noise. Therefore, let us choose a value in the middle: R7<4:0> = 01101 → $\frac{1}{14\times32\ \mu s}$ = 2232 b/s.

3.1.8 Envelope detector time constant

The AS3933 uses ASK modulation. Therefore, the envelope is extracted. This is done with the 'fast envelope' and its setting must be adjusted to the symbol rate. The symbol rate in this case is half the bit rate as described in section 8.5.1 DS → symbol rate = 1116 $\frac{Manchester\ symbols}{s}$. The closest value in Figure 6 (table 20 DS) is 1130 $\frac{Manchester\ symbols}{s}$ → R3<2:0> = 011.

Figure 6: Fast envelope settings

R3<2>	R3<1>	R3<0>	Symbol Rate [Manchester symbol/s]
0	0	0	4096
0	0	1	2184
0	1	0	1490
0	1	1	1130
1	0	0	910
1	0	1	762
1	1	0	655
1	1	1	512

3.1.9 Minimum required preamble length

The AS3933 takes the incoming ASK modulated signal as input and provides the digitized data stream as output. Thus, the signal is compared internally against a reference threshold which determines when the signal is a 'high' or a 'low'. The AS3933 offers two possibilities for this threshold: the dynamic threshold and the absolute threshold. The absolute threshold can be used in case the surrounding is not very noisy. It will automatically be set and does not require the preamble to settle to a specific value. The preamble can therefore be minimized.

The dynamic threshold uses the preamble to settle to a middle value. Thus, the preamble needs to be at least as long as specified in Figure 7 (table 21 DS) and at least 6 bit. With $T_{bit} = \frac{1}{2232} s$ the lower limit is 2.69 ms. Choosing 12 bit preamble instead of 6 this yields 5.376 ms for the preamble → R3<5:3> = 111.

Figure 7: Minimum required preamble lengths

R3<5>	R3<4>	R3<3>	Minimum Preamble Length [ms]
0	0	0	0.8
0	0	1	1.15
0	1	0	1.55
0	1	1	1.9
1	0	0	2.3
1	0	1	2.65
1	1	0	3
1	1	1	3.5

Additional settings that influence the digitization process are the comparator's hysteresis. It can be set to work only on positive signal edges and on both positive and negative. Moreover, the value of the hysteresis can be set to 20 mV or 40 mV. This is done with bits R3<7:6> as described in the datasheet in section 8.4.

3.1.10 Pattern correlation

As we are trying to make the system robust against noise we will allow the wakeup only on reception of the correct pattern. This requires the correlator to be enabled → R1<1> = 1. The pattern can be defined in registers R5<7:0> and R6<7:0>. We can decide whether the pattern stored in the register is the bit representation or symbol representation. The difference lies in the total number of available patterns and what the transmitter needs to send. In case the bit representation is used the pattern stored in registers R5 and R6 needs to be conforming to Manchester coding. Therefore, we can have a maximum of 2^8 = 256 different patterns. The transmitter in this case would need to transmit exactly the sequence stored in R5 and R6. For the case that the values represent Manchester symbols we can choose all 16 register entries independently. This gives us 2^16 = 65536 possible patterns. However, the transmitter needs to transmit 32 bits in this case. Let us use the bit representation and define a simple pattern: R6<7:0> = 01100110 and R5<7:0> = 01010101. Thus, our pattern will be: 6655 hex.

In section 8.6.2 it is mentioned that the preamble and pattern cannot be longer than 30 symbols for 16-bit pattern detection. Let us see if this restriction is met: preamble = 12 bit = 6 symbols; pattern = 8 symbols → 14 symbols.

With the pattern we can now decide whether to use the single wakeup pattern correlation or double wakeup pattern correlation. The difference is that for double wakeup pattern correlation the same pattern needs to be detected twice in a row. This will prolong the wakeup procedure and will not be enabled in this case → R1<2> = 0.

Finally, we do not want to have to decode the data with the µC. This is achieved by enabling the Manchester decoder → R1<3> = 1. The incoming Manchester encoded stream will be automatically decoded and can be used right away by the µC.

3.1.11 Automatic Time-Out

To terminate the wake-up state we have two possibilities: the µC sends the direct command ‘clear_wake’ or the automatic time-out function is used. The possible values for the automatic time-out range from 50 ms up to 350 ms as shown in Figure 8 (table 23 DS) and are set with register R7<7:5>. Let us use R7<7:5> = 010.

Figure 8: Automatic time-out settings

R7<7>	R7<6>	R7<5>	Timeout
0	0	0	disabled
0	0	1	50 msec
0	1	0	100 msec
0	1	1	150 msec
1	0	0	200 msec
1	0	1	250 msec
1	1	0	300 msec
1	1	1	350 msec

3.1.12 Artificial Wake-Up

The artificial wake-up feature regularly wakes-up the system with an interrupt signal that lasts 128 µs. This feature could be used to regularly get feedback on the surroundings and adjust settings. The artificial wake-up counter starts counting after the last successful wake-up event. If no successful wake-up happens during the time interval defined in register R8<2:0>, then the artificial wake-up is triggered. Otherwise, the counter is reset and begins counting again after the wake-up is terminated. Further details are given in section 8.1.2.

3.1.13 Automatic Gain Control AGC

The automatic gain control is used to automatically set the appropriate gain for the input stage. The amplifier’s (VGA) maximum gain is defined with the gain reduction settings in register R4<3:0>. The AGC starts to reduce the gain of the amplifier once the frequency detection was successful. It reduces the gain until the signal is within defined boundaries. Depending on how much the gain could be reduced – meaning the receiver sees a strong signal – the RSSI increases (the RSSI is the reciprocal of the amplifier’s gain).

The AGC can be controlled with registers R1<6:5> and R9<7>. Setting R1<6> will set a time limit for the AGC. It will then only be active for 256 µs after the frequency detection was successful.

Furthermore, it can be chosen to let the AGC only decrease the gain or also increase it again. In case the second option is chosen – i.e. R1<5> = 1 AGC operating in both directions – the gain can still not be increased above the value defined in the gain reduction settings.

R9<7> disables the AGC and the input will always work with maximum gain.

Besides the gain reduction settings the AS3933 also offers a +3 dB sensitivity boost. This boost can be enabled with register R2<5>.

Section 8.3.1 in the datasheet explains the use of the AGC. The default settings are not time limitation (R1<6> = 0), AGC working up and down (R1<5> = 1) and AGC enabled (R9<7> = 0).

3.1.14 Antenna Damper

The antenna damper is made up of resistors inside the chip that can be put in parallel with the antenna tank. A description is given in section 8.3.2 of the datasheet. It should be noted that the quality factor of the antenna tank will be decreased by activating the antenna damper. This will affect the maximum possible communication distance.

It can be desirable to achieve this effect, as described in section 12 for example, but in this case we do not want to have the damper enabled for standard operation: R1<4> = 0.

Figure 9: Possible values for the antenna damper

R4<5>	R4<4>	Shunt Resistor
0	0	1 kΩ
0	1	3 kΩ
1	0	9 kΩ
1	1	27 kΩ

3.2 Register settings

With the design decisions so far the below table can be put together. All other values that are not listed in this table use the default settings.

Figure 10: Register map

Parameter	Value	Setting
f_{carr}	125 kHz	R8<7:5> = 000
f_{RC}	31.25 kHz	R1<0> = 1, R2<6> = 0
T_{clk}	32 µs	
Frequency detection tolerance	Tight	R2<1:0> = 10
Scanning mode	Enable	R0<4> = 1
Channel 2	Disabled	R0<3> = 0
T_{burst}	3 ms	
Bit rate	2.232 kb/s	R7<4:0> = 01101
Symbol rate	1116 symbols/s	R3<2:0> = 011
Preamble length	5.376 ms	R3<5:3> = 111
Correlator	enabled	R1<1> = 1
Pattern extended to 32 bits	disabled	R0<7> = 0
Double wake-up pattern correlation	disabled	R1<2> = 0
Manchester decoder	enabled	R1<3> = 1
Pattern Byte 1	66	R6 = 01100110
Pattern Byte 2	55	R5 = 01010101
Automatic Time-Out	100 ms	R7<7:5> = 010

Parameter	Value	Setting
Artificial Wake-up	Disabled	R8<2:0> = 000
AGC	Enabled	R9<7> = 0
AGC	Operating in both directions without time limitation	R1<6:5> = 01
Gain reduction settings	No gain reduction	R4<3:0> = 0000
Sensitivity boost	Disabled	R2<5> = 0
Antenna damper	Disabled	R1<4> = 0
Capacitor bank channel 1	C = 16 pF	R17<4:0> = 10000
Capacitor bank channel 2	Not connected	R18<4:0> = 00000
Capacitor bank channel 3	C = 16 pF	R19<4:0> = 10000

3.3 Hardware design

The system is more or less completely defined by the decisions from the previous section. We now need to choose hardware that fits the requirements.

3.3.1 Antenna tank

The antenna tank of the AS393x should be designed as a parallel resonant circuit. There are receiver coils that are specifically designed for the low frequency bands such as the SDTR1103 by Premo. The resonance frequency of the antenna tank then needs to be tuned to the desired value using capacitors in parallel to the coil. The tank's quality factor can be adjusted with a parallel resistor.

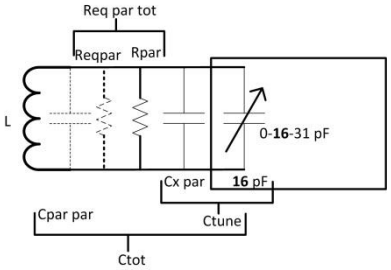
To help with the antenna tank design an excel sheet is available: AS3933_LCO_DESIGN_HELPER. It takes input arguments such as the coil's quality factor and inductance and calculates the required parallel capacitance and resistance based on the target resonance frequency and quality factor. This gives a good starting point for the design, which should then be fine-tuned with the help of measurements.

For the current example the coil SDTR1103-0720J could be used. Its parameters are:

- L = 7.2 mH @ 125 kHz
- C_{res} = 225 pF
- Q > 36 @ 125 kHz
- SRF > 350 kHz
- RDC = 105 Ohm max.
- Sensitivity = 75 mVpp/App/m @ 125 kHz

Inputting these parameters into the design helper sheet yields the following values for the circuit elements shown in Figure 11.

Figure 11: Antenna tank circuit



- $C_{par\ par} = \frac{1}{4\,\pi^2 SRF^2 L} = 28.72$ pF
- $C_{total} = \frac{1}{4\,\pi^2 f^2 L} \rightarrow C_{tune} = C_{total} - C_{par\ par} = 196.44$ pF
- $C_{x\ par} = C_{tune} - 16$ pF = 180.44 pF → this is the value that should be used when antenna tuning is implemented.
- $Q_{max} = \frac{2\,\pi\,f\,L}{R_{series}}$. In case the value for R_{series} is not given in the coil's spec, then the Q from the spec should be taken.
- $R_{eq\ par} = Q_{max}\sqrt{\frac{L}{C_{total}}} = 203.68$ kOhm → equivalent parallel resistor of the coil and capacitor circuit.
- $R_{eq\ par\ total} = \frac{R_{eq\ par} R_{par}}{R_{eq\ par} + R_{par}} = 144.72$ kOhm → R_{par} is the external resistor that is placed in the antenna tank, $R_{par} = 500$ kHz in this example.
- $Q = R_{eq\ par\ total}\sqrt{\frac{C_{total}}{L}} = 25.59$
- Maximum Bandwidth = $\frac{f}{Q} = 4.88$ kHz
- Maximum data rate = $\frac{maximum\ Bandwidth}{2} = 2442\ \frac{manchester\ symbols}{s}$

The maximum data rate that can be achieved theoretically with this setup is slightly bigger than the data rate that we want to use. This is a good starting point, from where the system can be optimized with measurements and tests.

3.3.2 Antenna tuning

The AS3933 offers the possibility to fine tune the antenna tank. It is therefore possible to use less expensive components and compensate for process variations. For each channel 31 pF additional capacitance is available inside the chip. Thus, designing the tank such that it is perfectly in tune when half of the internal capacitors are added will make it possible to compensate process variations both up and down. In Figure 10 16 pF are already put in parallel to channels 1 and 3. Note that when antenna tuning is not used or the channel is deactivated the capacitor bank should be deactivated as well. Section 8.9 of the datasheet gives some details on the tuning procedure.

When the antenna tuning is implemented there are some things that should be considered. First of all, the antenna tuning works the following way: the chosen channel is connected to an internal LC oscillator and the resulting signal put out on the DAT pin. The µC then needs to measure the frequency of this signal and determine whether it is where it should be or not. Thus, the antenna tuning will only be as accurate as the microcontroller's time base.

The next issue is cross coupling between channels when more than one channel is used. To reduce this effect the internal antenna damper resistor can be activated. Yet, we need to be careful to not degrade the quality factor of the antenna tank too much. The complete $R_{eq\ par\ total}$ needs to be greater than 10 kOhm, otherwise the internal LC oscillator will not oscillate. As all of the resistors are in parallel, and the other values we calculated are far bigger than what we can add internally, the internal resistor will determine $R_{eq\ par\ total}$.

With these thoughts in mind let us begin the tuning. The first thing we'll do is to enable the internal 27 kOhm resistor → R4<5:4> = 11. Then the LC oscillator needs to be connected to a channel. We are using channel 1 and 3. Let's start with channel 1 → R16<2:0> = 001. Now there should be a signal on the DAT pin. Measuring this signal the µC needs to decide whether it is above f_{carr}, below or right at it, and change the value of register R17 correspondingly. This procedure should be repeated until the optimum value is reached.

The same procedure then needs to be repeated for channel 3.

3.3.3 Crystal Oscillator

A crystal usually requires a specific load capacitance at its terminals in order to oscillate at the correct frequency. There are various application notes that describe an oscillator's circuit and how to calculate these values. One example would be the application note AN826 by Microchip.

A common way to calculate the load capacitance uses the following equation: $C_L = \frac{C_2 C_3}{C_2 + C_3} + C_S$. Here C_L denotes the load capacitance that is given in the crystal's spec, C_2 and C_3 the capacitance that is placed on the PCB, and C_S the parasitic capacitance due to routing, chip input and other parasitic effects. The capacitors C_2 and C_3 can be set equal.

Measuring the oscillator's frequency is usually not a simple task. Simply putting scope probes on the terminals will add additional parasitic capacitance and will pull the frequency to a different value. The AS3933 offers the possibility to measure the oscillator frequency on one of the chip's pins. In this way it is possible to easily verify that the frequency is where it should be. How this is done will be explained in section 3.4.

The crystal spec is not the only thing that needs to be taken into consideration when designing the oscillator. The AS3933 also puts some restrictions on what it can handle. Characteristics that the quartz needs to fulfill so the AS3933 can operate it are given in table 27 of the datasheet.

3.4 Verifying the design

3.4.1 Antenna tank

The resonance frequency and the quality factor of the antenna tank are best measured with a network analyzer. The tuning capacitor values and resistor value can then be adjusted to achieve the optimum tuning. During production the antenna tank can be fine-tuned as described in section 12. This can also be used as quality test: in case the antenna tuning cannot be completed successfully, there is an issue with the unit.

3.4.2 Oscillator

As mentioned before it's difficult to measure the oscillator frequency by just putting a scope probe on the crystal. The extra load capacitance will influence the oscillator's frequency and the result will not be satisfying. The AS3933 can be configured to put the oscillator frequency on the CL_DAT pin.

This can be done by setting R2<3:2> = 11 and R16<7> = 1. As the signal is decoupled from the crystal itself, additional capacitance on the CL_DAT pin will not influence its oscillation.

The same method can be used with the internal RC oscillator or a different external source to verify that the clock signal is at the correct frequency.

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