AS6040

External Amplifier Application Note

AS6040 with external amplifier

Revision: 3
Release Date: 2021-06-29

Content Guide

1 Introduction

The AS6040 ultrasonic flow converter is dedicated to measurements of gas flow. Therefore, a charge pump has be integrated to increase the fire voltage up to 17 V and in addition a programmable gain amplifier (PGA) is integrated to amplify the receive signal with up to 136 V/V.

Of course, the receive amplitude depends on the sensor design, the transducers and also the gas medium. When working with natural gas the amplitude is typically reduced by 50% compared to air. As a consequence, we see applications where the gain of the internal PGA is not enough and where we need an additional external amplifier.

This application note shows how to add an external 1-stage or 2-stage amplifier to the AS6040 to achieve a gain of up to 250 V/V.

Investigation have been made with the version v2.0 of the reference board AS6040-QF_DK_RB.

2 Description

The AS6040 has an internal programmable gain amplifier (PGA). The signal quality for a gas meter with AS6040 depends on the charge pump voltage and in combination with the PGA gain. The gain is limited with regard to the bandwidth of the amplifier. The highest gain of the internal PGA is 96 V/V at 200 kHz and 69 V/V at 500 kHz. When the gain of the internal PGA is not high enough the signal quality can be improved with an external amplifier. For a gas meter application, the amplitude at air should be between 400…500 mV as the amplitude can be halve with natural gas due to the higher attenuation of the gas medium.

The application note shows two approaches for implementing external amplifiers with the AS6040. One solution is for a single external amplifier when a gain <125 V/V is sufficient and a second solution works with a 2-stage amplifier design for gains up to 250 V/V. It should be a voltage feedback (VFB) operational amplifier. The amplifiers should have a low offset, low noise and a gain bandwidth of 30…300 MHz. Within a 2-stage amplifier design the bandwidth can be smaller from 15 to 60 MHz. It should be optimized for low voltage single supply and rail-to-rail output characteristic. The supply current should be appropriate for low power applications (Icc < 3 mA) and should have a power down or power saving mode. For ultrasonic sensor applications the following amplifiers can be considered, but others may also be adequate.

- LMP7711, GBW = 14 MHz, Texas Instruments, https://www.ti.com/
- SGM8967-3, GBW = 27 MHz, www.sg-micro.com/
- LTC6261, GBW = 30 MHz, Analog Devices, https://www.analog.com
- MAX44280, GBW = 50 MHz, Maxim Integrated, https://www.maximintegrated.com/
- OPA835, GBW = 56 MHz, Texas Instruments, https://www.ti.com/
- LT6233, GBW = 60 MHz, Analog Devices, https://www.analog.com
- ADA4807, GBW = 105 MHz, Analog Devices, https://www.analog.com
- OPA836, OPA837, OPA838, GBW = 118 … 300 MHz, Texas Instruments, https://www.ti.com/
- LTC6246, GBW = 180 MHz, Analog Devices, https://www.analog.com

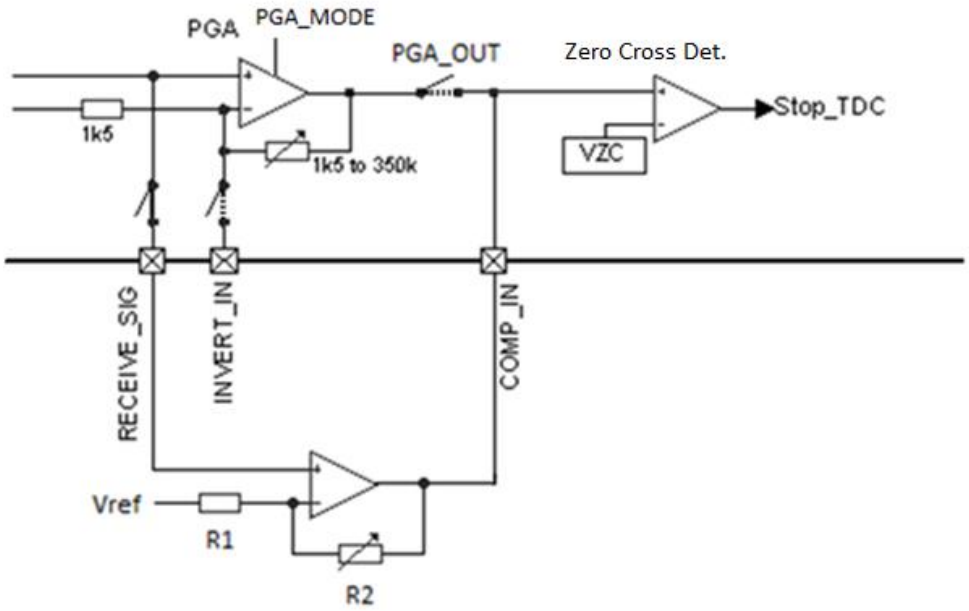
2.1 Functional Description

The external amplifier is connected between the AS6040 RECV_SIG and COMP_IN pin. We recommend using the amplifier in a non-inverting configuration same as the internal PGA. The circuit schematic of AS6040 with external amplifier is shown in Figure 1. To use the external amplifier some changes in the gas meter default configuration must be done. The internal PGA must be disabled in the configuration register **CR_USM_AM** option PGA_MODE (0xCB bit-21 = 0).

Also the switch between the PGA and the comparator input for the TDC must be opened to avoid signal distortions, in **CR_USM_PRC** option TI_PGA_CON_MODE[0] (0xC8 bit-30 = 1). The receive signal is connected to the RECV_SIG pin with the internal switch in **CR_TRIM3** register (0xCE bit-29 = 1). The INVERT_IN pin which is normally used with the PGA and the T-filter can be opened in **CR_USM_PRC** with TI_PGA_CON_MODE[1] (0xC8 bit-31 = 0).

The output voltage level of the external amplifier at the COMP_IN pin should be at VRef of 700 mV within ±10 mV. This must be considered during the design and testing phase of the circuit. When the voltage level is outside of this range the amplitude measurement has an error and the FHL range is reduced.

Figure 1: Schematic diagram of AS6040 with external amplifier



The gain setting of the external amplifier is done with the resistors R1 and R2. The following formula describes the gain of a non-inverting amplifier:

Equation 1:

$$G = \frac{R2}{R1} + 1$$

The resistor R1 can be chosen in the range of 510 ohms to 1.5 kΩ. To reach a higher gain as with the AS6040 PGA the gain should be set between 80 V/V to 150 V/V.

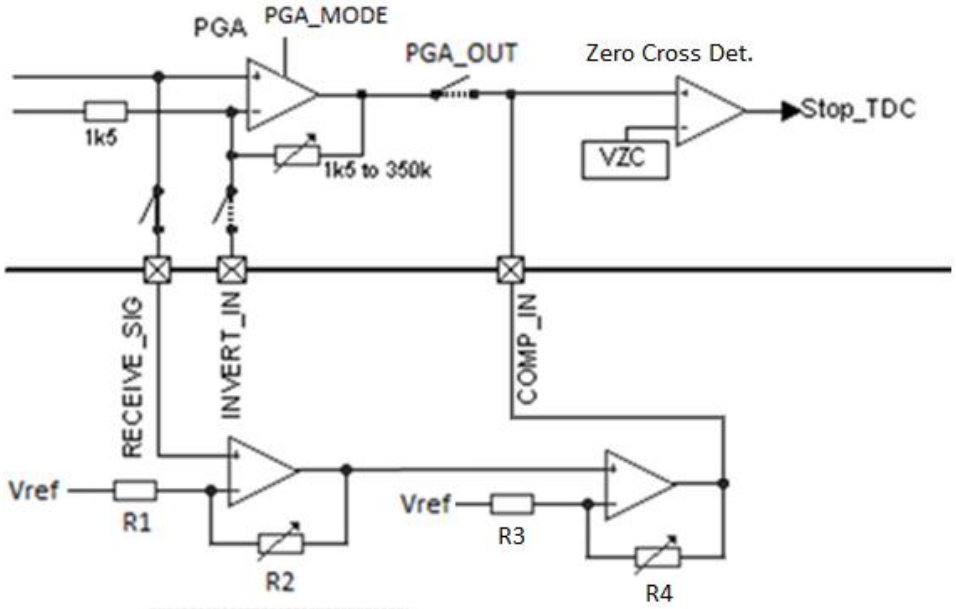
Therefore, choose the resistor R2 in the range of 27 kΩ to 120 kΩ. The following table in Table 1 shows some resistor combinations and their gain. Depending on the amplifier gain bandwidth consider that the highest gain is not reachable with every amplifier. To reach high gains with a single amplifier stage it is recommended to use amplifiers with a gain bandwidth higher than 50 MHz.

Table 1: Exemplary gain settings of non-inverting amplifier with R1 = 1 kΩ.

Resistor R2 in kΩ	Gain in V/V	Gain in dB
68	69	36.78
82	83	38.38
100	101	40.08
120	121	41.65
150	151	43.58

If a single high bandwidth amplifier cannot be used in the design or the reachable gain is not sufficient, we present a circuit with external amplifiers in a 2-stage design for the AS6040. The circuit in Figure 2 shows a 2-stage design. In a 2-stage design the gain of each single stage can be lower and therefore it enables the usage of amplifiers with mid-range gain bandwidth of 14 to 60 MHz. But it is also possible to set up a combination of a high bandwidth amplifier and high gain in the 1st stage and a mid-range amplifier and low gain in the 2nd stage.

Figure 2: Schematic diagram of AS6040 with 2-stage external amplifier



If both stages should have the same gain in the 1st and 2nd stage choose R1 = R3 and R2 = R4. The noise performance is better if the gain in the first stage is higher than in the second stage. It is recommended to choose the gain in the first stage as high as possible but take care that it isn´t at the bandwidth limitation of the amplifier. The gain of each stage can be calculated with Equation 1. The overall gain of the 2-stage amplifier design is in Equation 2.

Equation 2:

$$G_{all} = Gain_{1st\ stage} \cdot Gain_{2nd\ stage}$$

The following table in Table 2 shows some resistor combinations for gain settings between 160 V/V and 230 V/V. The first stage has a high gain and the second stage sets the final gain with a small gain.

Table 2: Exemplary gain settings for a 2-stage amplifier design with high gain (1st stage) combined with low gain in 2nd stage. For R1 = R3 = 510 ohms.

R2 in kΩ	Gain in V/V 1st stage	R4 in kΩ	Gain in V/V 2nd stage	Overall gain in V/V	Overall gain in dB
39	77.4	0.56	2.09	162.4	44.21
39	77.4	0.68	2.33	180	45.12
39	77.4	0.82	2.6	201. 8	46.10
39	77.4	1	2.96	229.1	47.2

To use a high-bandwidth amplifier a different circuit design approach is needed. The operational amplifiers with high bandwidth have typically a high input bias current I_b in the range of 0.1 µA to 5 µA due to the semiconductor technology. The bias current through the input terminals of the amplifier can shift the ultrasonic transducer reference level slightly. This would to a relatively high deviation from Vref at the output which could exceed the allowed voltage range at the COMP_IN input. Therefore is the negative input decoupled with a capacitor C1 to prevent that the DC level at the output is not shifted too much. The circuit is shown in Figure 3 with a capacitor C1 connected between R1 and GND. The capacitor also limits the bandwidth for the signal at low frequencies. The circuit has a pole f_P and a zero-frequency f_G due to the capacitor C1.

Equation 3:

$$f_G = \frac{1}{2\pi C_1(R_1 + R_2)} \qquad and\ f_P = \frac{1}{2\pi C_1 R_1}$$

The zero-frequency f_G is the +3 dB corner frequency at unity gain. The pole-frequency f_P is the -3 dB cutoff frequency at the gain defined by R1 and R2.

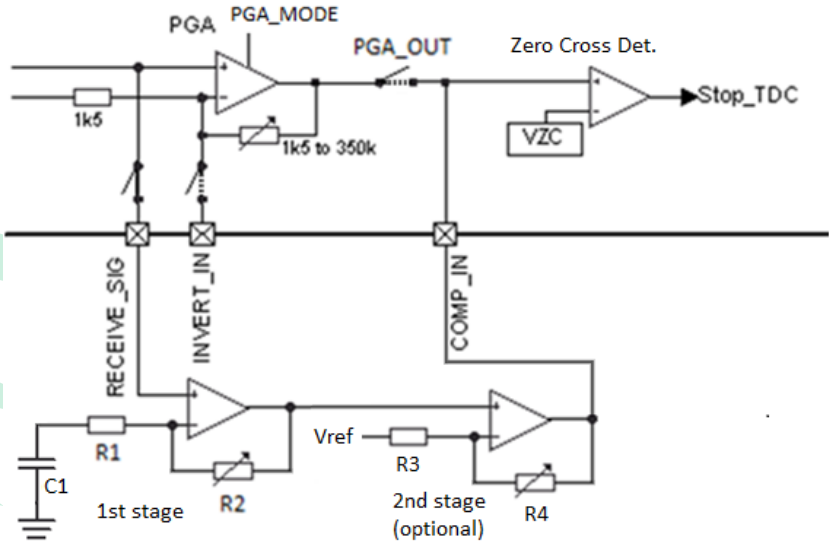
Choose C1 with the following values:

200 kHz transducers: C1 = 330 to 470 nF

500 kHz transducers: C1 = 100 to 220 nF

The circuit in Figure 5 can also be used for standard CMOS amplifiers with very low input bias currents and gain bandwidth product between 14 MHz and 50 MHz. The noise performance of the TOF values can then be slightly better compared to the circuit in Figure 2.

Figure 3: Schematic diagram of AS6040 with external 2-stage amplifier and AC decoupled inverting input



The amplifier with the high-bandwidth should have a high gain in the first stage. If the gain of the first stage itself is not sufficient a second stage can be added and has a low gain of 2 V/V to 6 V/V. In the table in Figure 6 are some exemplary values for the amplifier circuit listed. The resistor values for the high-bandwidth amplifier are smaller because of the high bias current. This limits the noise contribution and reduces the offset at the output.

Table 3: Exemplary gain settings for a 2-stage amplifier design with high gain (1st stage) combined with low gain in 2nd stage. For R1 = 10 Ω and R3 = 1 kΩ.

R2 in kΩ	Gain in V/V 1st stage	R4 in kΩ	Gain in V/V 2nd stage	Overall gain in V/V	Overall gain in dB
0.51	52	1.5	2.5	130	42.28
0.51	52	2.2	3.2	166	44.42
0.51	52	2.7	3.7	192	45.68
0.75	76	1	2	152	43.64
0.75	76	1.5	2.5	190	45.58
0.75	76	1.8	2.8	212.8	46.56
0.82	83	1.0	2	166	44.4
0.82	83	1.2	2.5	207.5	46.34
1.0	101	1.0	2	202	46.11
1.0	101	1.2	2.2	222.2	46.93

Important:

DC-Voltage level at COMP_IN

It is important to check that the signal level at the output of the amplifier at the COMP_IN pin is close to the Vref level of 700 mV. The offset between these two signals should not exceed 10 mV. Else the amplitude measurement error gets greater than the specified 10 mV in the datasheet.

AC decoupling of external amplifier circuit

Thinking about amplifier circuits for amplification with specific transmission frequency of the signal would also lead to circuits with AC decoupled path between the ultrasonic transducers and the comparator. Such circuits are not proposed for the AS6040 as the switching of the receive signal is not synchronized with the amplifier circuit. The reloading time of the coupling capacitors

in the frequency range of 150 kHz to 550 kHz is too long and increases the power consumption too much for battery supplied applications.

For the receive signal processing with the comparator only the carrier frequency of the transducers are from interest. As active bandpass filter circuits are limited in the gain and such a circuit design can consist of up to four amplifier we didn´t present such a circuit.

2.2 Zero-Cross Calibration (ZCC)

The zero-cross detection module maintains that the first hit level (FHL) at the comparator is added to the actual level at COMP_IN. Therefore, measures the ZCC the DC level at COMP_IN (pos. comparator input) and compensate it for the neg. comparator input. After the calibration the TDC can measure the receive signal at the zero-crossing which should be at the V_{ref} level of 700 mV. The output level of an amplifier can have an additional offset voltage higher or lower than V_{ref} depending of the temperature and the amplifier characteristics combined with the external gain setting.

Important note: It is important to verify that the ZCC is working with the external amplifier. The amplitude measurement of the receive signal is reference to the V_{ref} level. So, any offset from the V_{ref} level leads to an error in the amplitude measurement result. Therefore, we recommend a output level of the amplifier at COMP_IN DC-level of 700 mV ±10 mV, so that the error stays in an acceptable small range.

Troubleshooting with the ZCC:

Depending of the turn-on timing of the amplifiers and stabilization of the output signal we observed combinations where the ZCC is done before the circuit reaches a steady state. The deviation of the ZCC results are then too high and can also trigger an error flag (EF_ZCC_ERR). You can check the ZCC value in register SHR_ZCD_LEVEL (0xD9). It is scaled with a LSB value of around 0.88 mV. Which is a hex value between 0x31B and 0x321.

1. Power on: After power on the AS6040 makes always an initial ZCC calibration. When the chip is operating without an activated bootloader than there is no valid configuration (only the reset state of the CR registers). Depending on the circuit with the external amplifier the ZCC value can be not valid or wrong.
2. Unstable ZCC results: For the ZCC the amplifier can be turned on with the US_BUSY signal at GPIO4. Alternatively, it is also possible with the RECV_PATH_EN signal at GPIO5 (0xC2 bits 20:21 = 00; bits 22:23 = 11) combined with enabled receive path during ZCC, CR_TRIM1 bit 4 = 1. But this must be verified if there are not too much oscillations from the transducers at the signal.

3. Workaround in case no stable ZCC results are possible: If the ZCC result is not stable at all it would be possible to disable the ZCC completely and overwrite the SHR_ZCD_LVL register (0xD9) with the equivalent value measured at COMP_IN. This operation mode should only be used with a FHL regulation and phase modulation detection. Contact the Sciosense support.

2.3 Power Consumption and Amplifier Enable/Shutdown

To optimize the power consumption the amplifier can be put in a power down mode. The amplifier will only turned to active mode when a ultrasonic measurement or a zero-cross calibration (ZCC) is done. The power down current of the amplifier should be <1.5 µA to save current in a battery design. The amplifier will only be enabled when the receive signal is switched to the comparator. This is after the fire burst is sent until the last TOF hit is measured. Therefore, use the GPIO5 output with the **RECV_PATH_EN** signal.

The GPIO4 **Ultrasonic Measurement Busy** signal can also be used but offers less stability of DIFF_TOF over temperature and has a higher power consumption as the amplifier out is in saturation at V_{cc} level as long as the receive path is not switched to the comparator. The GPIO4 is an option for enabling the amplifier during the ZCC. Configure the GPIO4 as an output. During the ultrasonic measurement this signal enables the amplifier before the fire burst is sent until end of the amplitude measurement after the ultrasonic measurement. A summary of the GPIO functions for enabling external amplifier is in Table 4.

Table 4: AS6040 GPIO functions for amplifier enable/shutdown

GPIO	Name	Description	Config. Reg.
4	Ultrasonic Measurement Busy	During the ultrasonic measurement this signal enables the amplifier before the fire burst is sent until end of the amplitude measurement after the ultrasonic measurement. And is also high during ZCC.	**CR_GP_CTRL** 0xC2 bit-16:17 = 00, bit-18:19 = 01
5	RECV_PATH_EN	The amplifier will only be enabled when the receive signal is switched to the comparator. This is after the fire burst is sent until the last TOF hit is measured.	**CR_GP_CTRL** 0xC2 bit20:21 = 00, bit-22:23 = 11
5	RECV_PATH_EN during ZCC	The ZCC features a mode where the receive path with the transducer is switched to the comparator. Attention: Some transducer can be stimulated which disturbs the ZCC process.	CR_TRIM1 0xCC bit-4 = 1

To use both GPIO4 and GPIO5 for enabling the amplifier we provide a sample firmware code for the AS6040 CPU. The firmware takes over the control of the ZCC and high-speed clock calibration (HCC) and configures the GPIOs. The user can therefore define the measurement rate for the ZCC and HCC in the firmware data memory. After the defined number of ultrasonic measurements are done the firmware switches every time the GPIOs and initiates the ZCC and HCC.

The firmware assembler demonstration code can be found at the AS6040 product page of the Sciosense homepage.

2.4 Sample measurement single stage amplifier

The following example shows the measurement result with a single high-bandwidth amplifier (TI OPA838). The gain is set to 126 V/V. (R1: 12 ohms; R2: 1.5 kΩ; C1: 100 nF). We used gas transducers f = 500 kHz with a ToF_Sum of 250 µs at air.

In Figure 4 is the screenshot of the measurement. At channel 1 is the amplified receive signal measured at COMP_IN. The DC level is around 700 mV which is the V_{ref} level of the device. The amplifier is enabled 10 us after the fire burst ends. In Figure 5 is a sample TOF measurement result of the measurement shown in the oscilloscope screenshot. It is the Diff_TOF with a configuration of 10 TOF_HIT_SUM_NO.

Figure 4: Sample gas measurement with single amplifier and gain of 126 V/V.
1: COMP_IN; 3: US Fire Burst; 4: GPIO5 Receive port enable

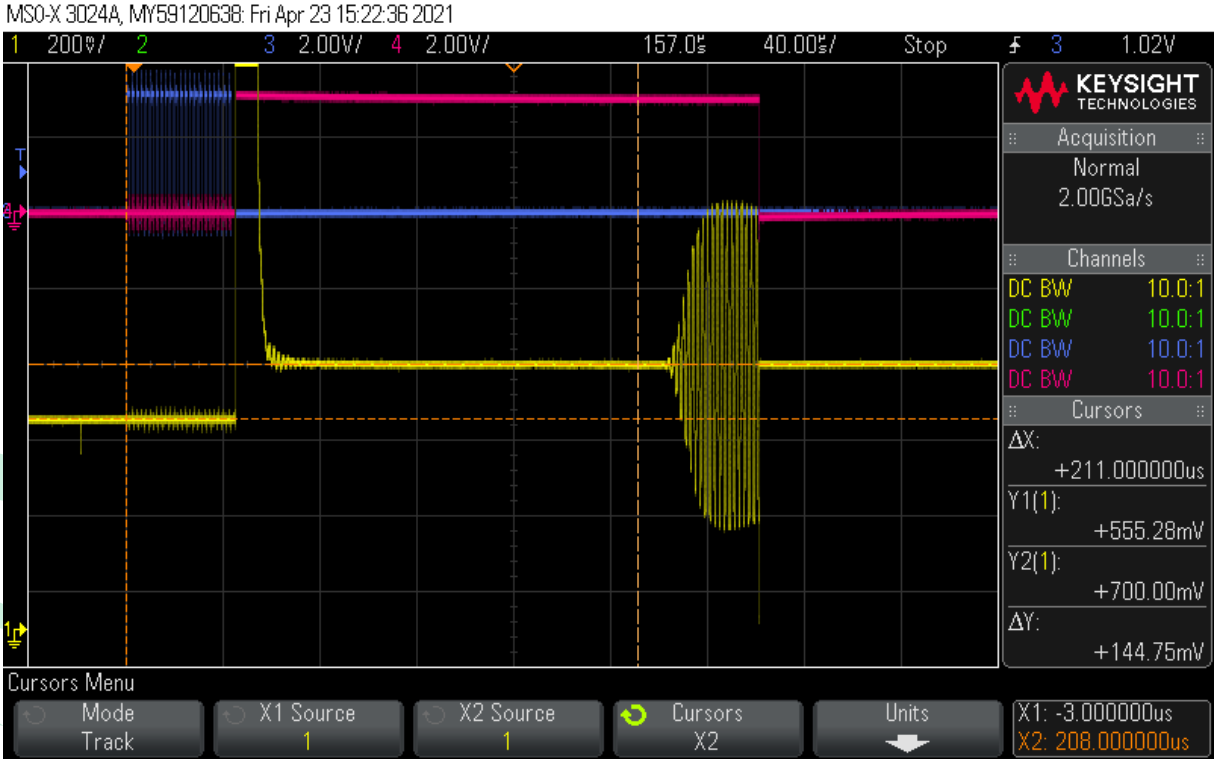
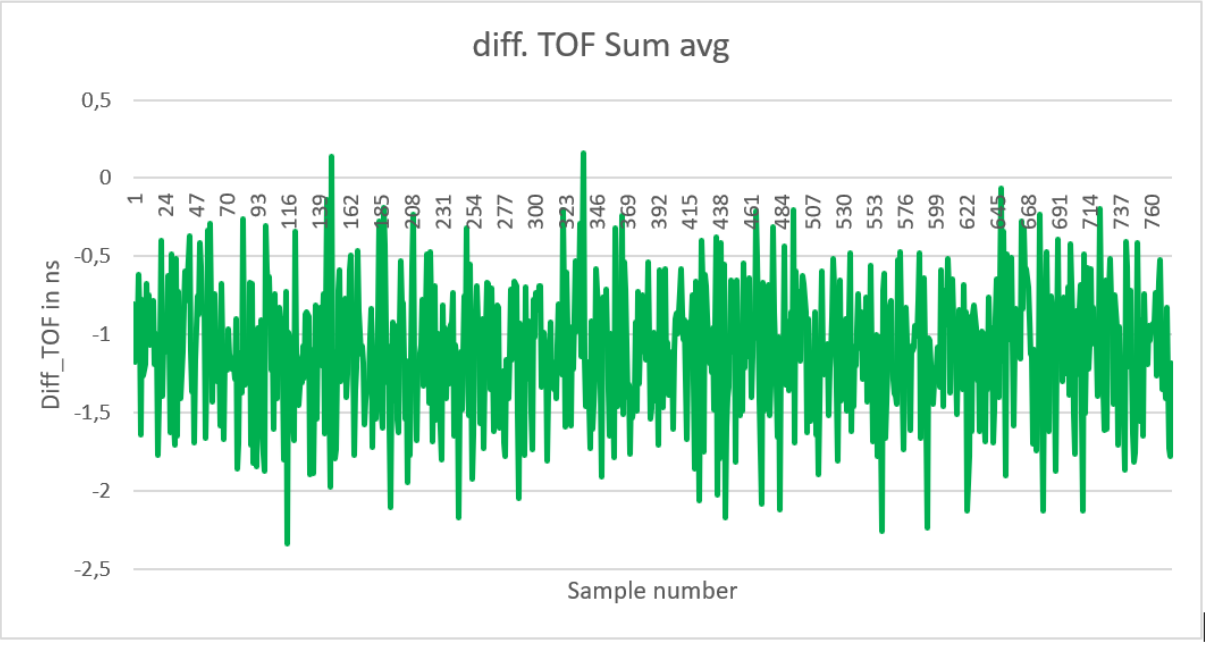
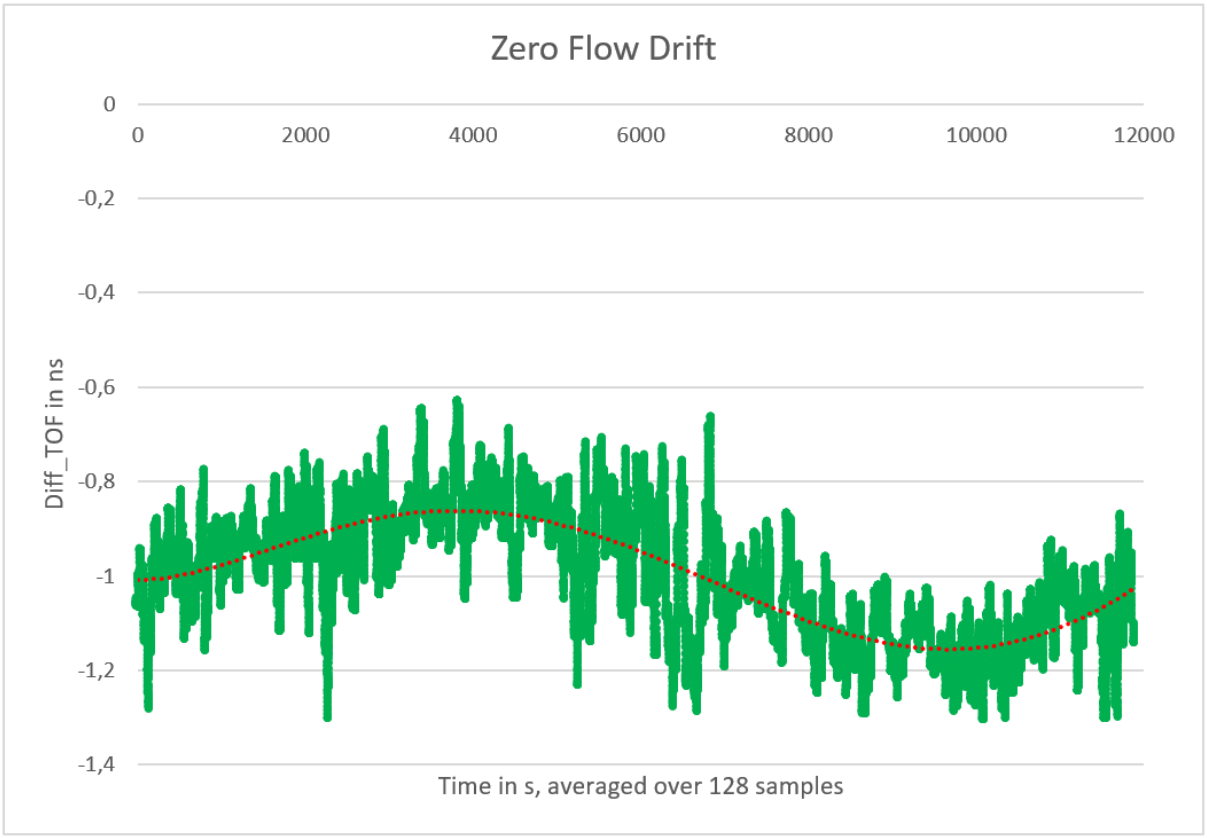


Figure 5: Measurement result with single amplifier of diff TOF. The standard deviation over 100 samples is around 410 ps.



The zero-flow drift over temperature was tested in a climate chamber. The demo board with the AS6040 and the external amplifier circuit was in the oven whereas the spool piece was at room temperature. The temperature cycle applied was starting from room temperature to -20 °C up to +40 °C and back to room temperature. The averaged result of the DIFF_TOF zero flow is in Figure 6.

Figure 6: Zero-flow drift test with single amplifier over temperature range of -20 to 40 °C. The curve is the DIFF_TOF averaged over 128 samples.



2.5 Sample measurement 2-stage amplifier

The following example shows the measurement result with 2 amplifiers (SG Micro SGM8967-3). The overall gain is set to 160 V/V. The first stage has a gain of 28 V/V and the 2nd stage has a gain of 5.7 V/V. (R1: 10 Ω; R2: 270 Ω; C1: 100 nF; R3: 1 kΩ; R4: 4.7 kΩ). We used gas transducers f = 500 kHz with a ToF_Sum of 250 us at air.

In Figure 7 is the screenshot of the measurement. At channel 1 is the amplified receive signal measured at COMP_IN. The DC level is around 700 mV which is the V_{ref} level of the device. The amplifier is enabled 10 us after the fire burst ends. In Figure 8 is a sample TOF measurement result of the measurement shown in the oscilloscope screenshot. It is the Diff_TOF with a configuration of 10 TOF_HIT_SUM_NO.

Figure 7: Sample gas measurement with 2-stage amplifier design and gain of 160 V/V.
1: COMP_IN; 2: Output 1st stage 3: US Fire Burst; 4: GPIO5 Receive port enable

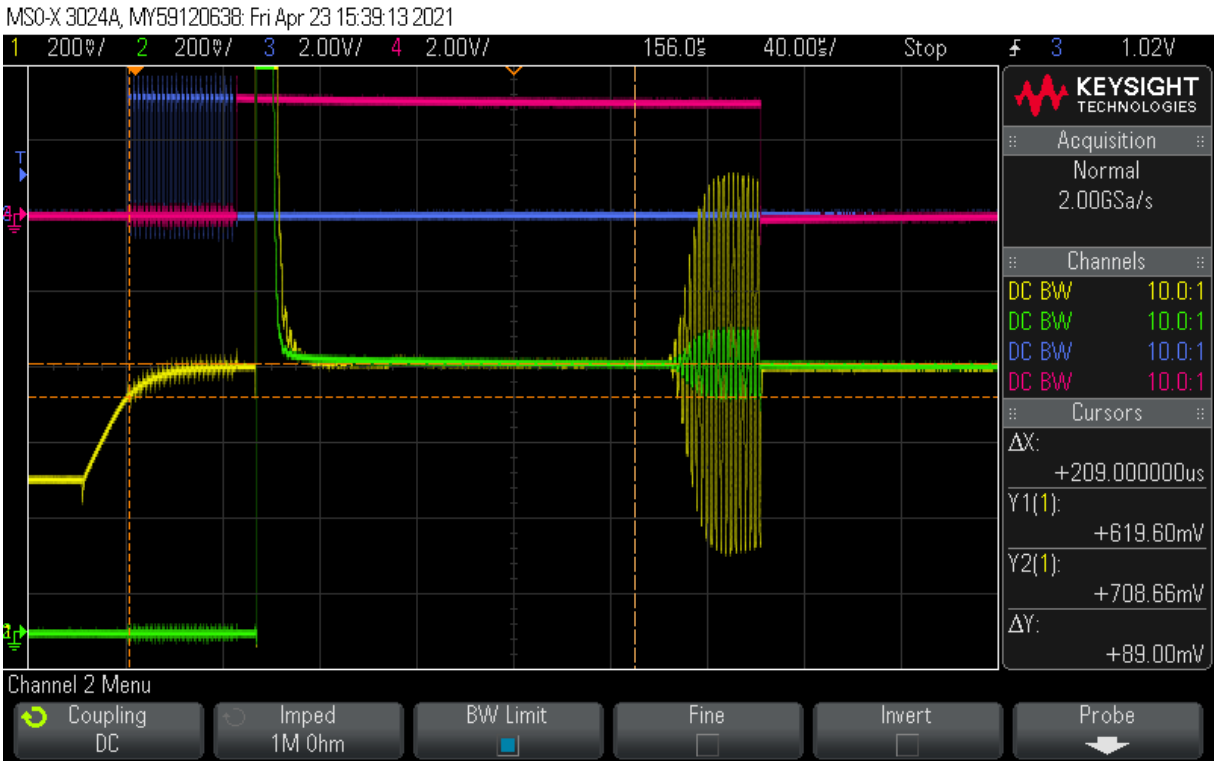
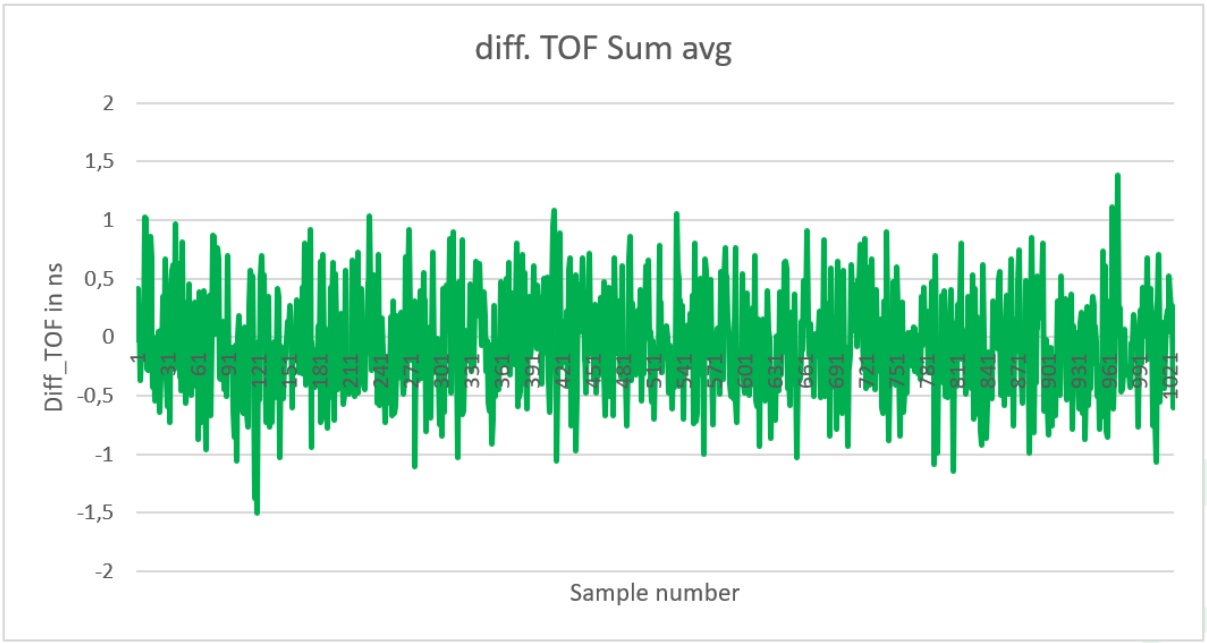


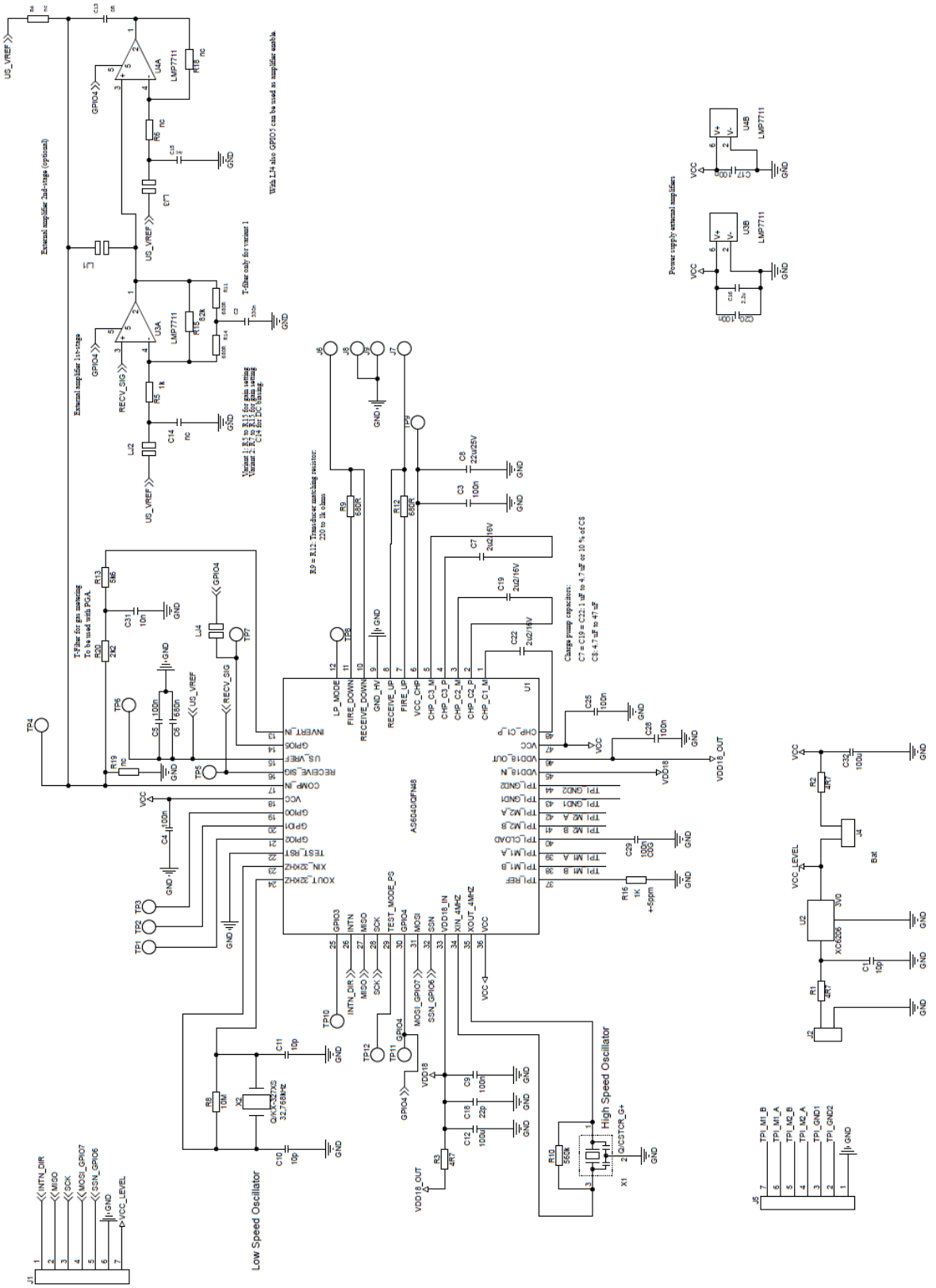
Figure 8: Measurement result with 2-stage external amplifier. The standard deviation over 100 samples is around 428 ps.



2.6 Schematic

The schematic for the AS6040 demoboard with external amplifier is shown in Figure 9.

Figure 9: Schematic of AS6040 demoboard v2.0 with external amplifier



2.7 Layout

For the layout of the analog signals take care about the signal integrity. At the board layout place the amplifiers near at the pins RECV_SIG and COMP_IN.

For the layout of the external amplifier refer to the recommendations for the amplifier part manufacturer. Keep the sensitive signal traces as short as possible and place the decoupling capacitors for the amplifier near at the supply pins.

The layout of the demo board can be found in the documentation of the AS6040 design kit.

Sometimes it may make sense to choose a FHL using narrower clearance range. This may improve stability over temperature variations.

2.8 Configuration of AS6040 with external amplifier

Default configuration AS6040 for 500 kHz transducer with external amplifier:

```
0x48DBA399   ; CR_WD_DIS Register
0x00800401   ; CR_IFC_CTRL Register
0x00C11111   ; CR_GP_CTRL Register
0x00000007   ; CR_USM_OPT Register
0x010FFFFF   ; CR_IEH Register
0x3946EC08   ; CR_CPM Register
0x19012100   ; CR_MRG_TS Register
0x00240000   ; CR_TPM Register
0x406E0064   ; CR_USM_PRC Register
0x60160208   ; CR_USM_FRC Register
0x010FEA10   ; CR_USM_TOF Register
0x2380DE81   ; CR_USM_AM Register
0x94A0C46C   ; TRIM_1 Register
0x401100C4   ; TRIM_2 Register
0x20A7400F   ; TRIM_3 Register
0x00000001   ; SHR Register 0xD0 ; TOF RATE
0x00003E80   ; SHR Register 0xD1 ; Multihit Release
0x00003E80   ; SHR Register 0xD2 ; Multihit Release
0x00000023   ; SHR Register 0xDA ; 1st Hit Lvl Up
0x00000023   ; SHR Register 0xDB ; 1st Hit Lvl Dn
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4 Document Status

Table 5: Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice.
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice.
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade.
Datasheet (Discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs.

5 Revision Information

Table 6: Revision History

Revision	Date	Comment	Page
0.9	2019-Dec-11	Initial Version	
1	2021-Jan-08	Transfer to ScioSense format Section 1.1 added	All 7
2	2021-Jun-29	Introduction text changed, typo corrections	

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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