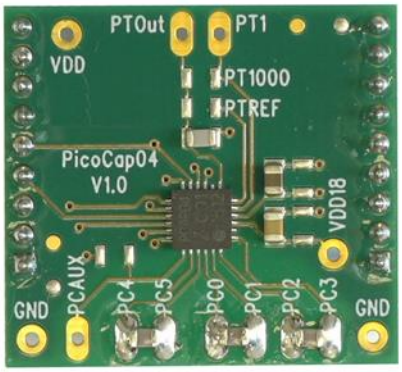

PCap04

Timing Aspects

PCap04 Application Note

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Content Guide

1 Introduction

PCAP04 is a capacitance-to-digital converter (CDC) based on discharge time measurements. It has an integrated digital signal processor (DSP) for on-chip data post-processing.

This application note describes how to set the timing and how to evaluate the duration of a complete measurement, including the data readout. In principle, the behavior is the same for PCAP02 and quite similar for the PCAP01.

In the following we use timer triggered conversion mode for all our discussions (C_TRIG_SEL = 2 / CONV_TIME > 0). Figure 1 shows the basic flow diagram of the whole sequence.

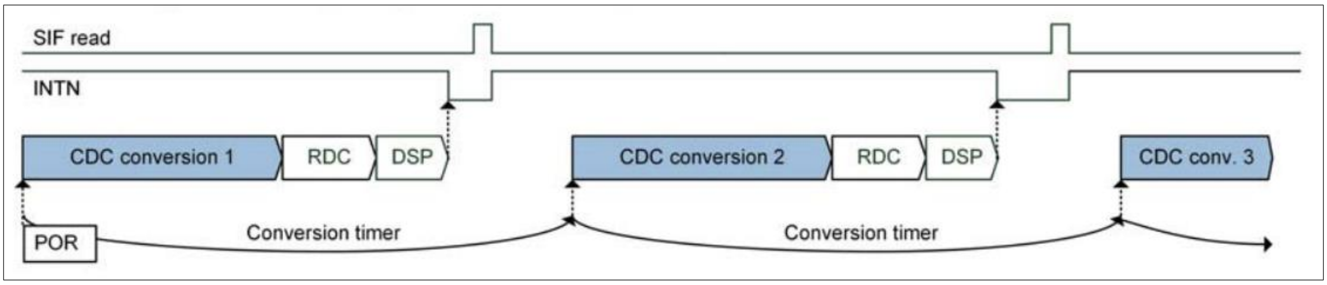

Figure 1: Conversion Mode

2 Preparation

2.1 Measuring Equipment

We use our PCAP04-DEV-KIT together with our evaluation software. The signals are captured by means of an oscilloscope. Note that any probe connected disturbs the CDC/RDC measurement with additional offset. But it is needed to see the real signals.

Based on the particular configuration, the probe is connected to corresponding input pin for …

- CDC measurement, CDC port, PCx (x = 0..5)
- RDC measurement, RDC port, PT0REF, PT1
- Interrupt, PG4, PG5
- Communication interface (SPI / I2C)

It is recommended to look at the output PCAUX to see the complete CDC sequence in one graph. This pin needs to be enabled before in the GUI: Expert Tab -> CDC Tab:

- RDCHG_INT_EN (Enable internal discharge resistors by default)
- RDCHG_EXT_PERM (Activate auxiliary Port PCAUX permanently for permanently discharge)

For a complete view of the RDC sequence use pin PTOUT.

2.2 Important Parameters

The main parameters for the timing of the CDC measurement are set in the cycle control:

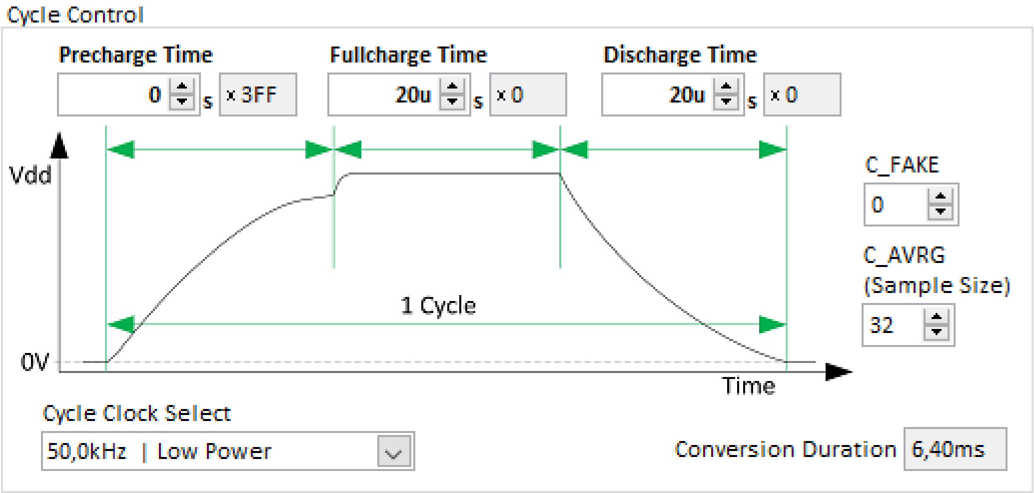

Figure 2: CDC Tab (Cycle Control)

For the RDC measurement similar settings are available:

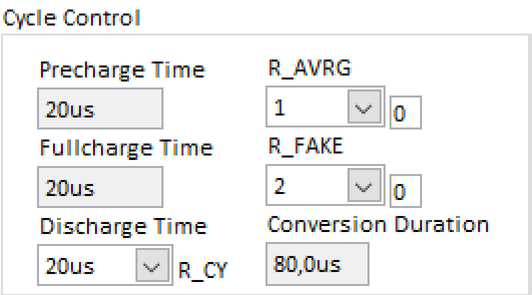

Figure 3: RDC Tab (Cycle Control)

The minimum value for the CDC cycle times depends on the base clock, which can be selected between the LF (10 to 200 kHz) and HF clock (2 MHz):

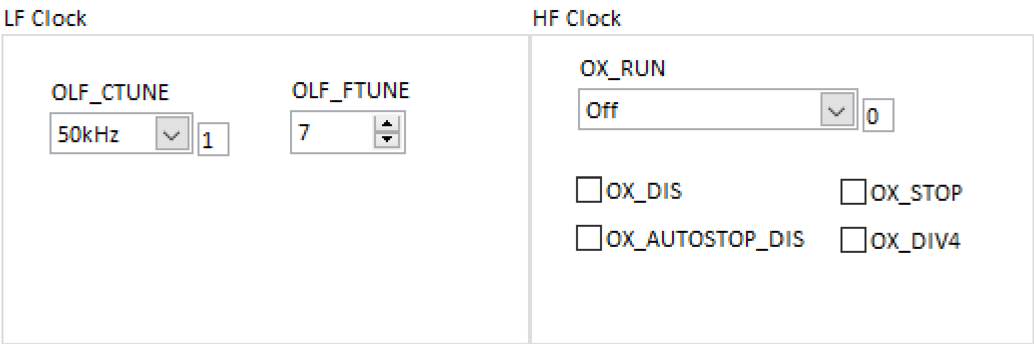

Figure 4: MISC Tab (LF Clock / HF Clock)

Settings for the DSP are made here:

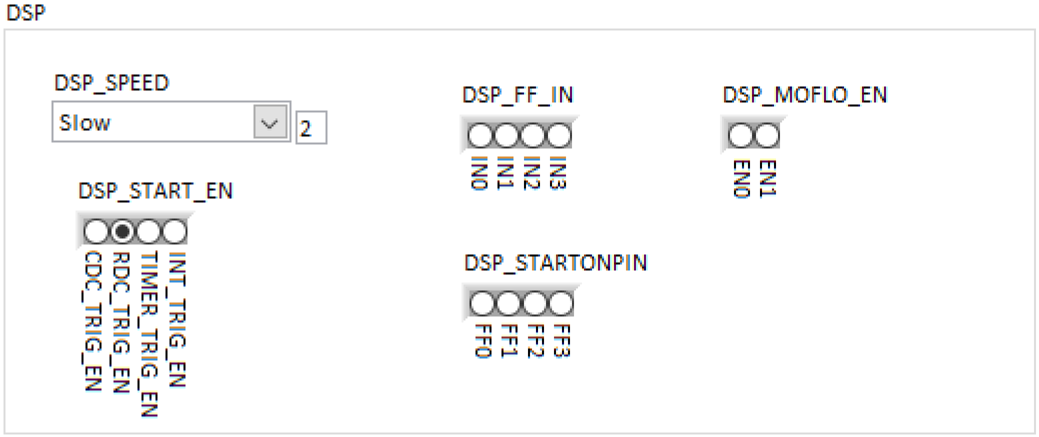

Figure 5: DSP/GPIO Tab (DSP)

The PCAUX pin is enabled and configured under the expert tab.

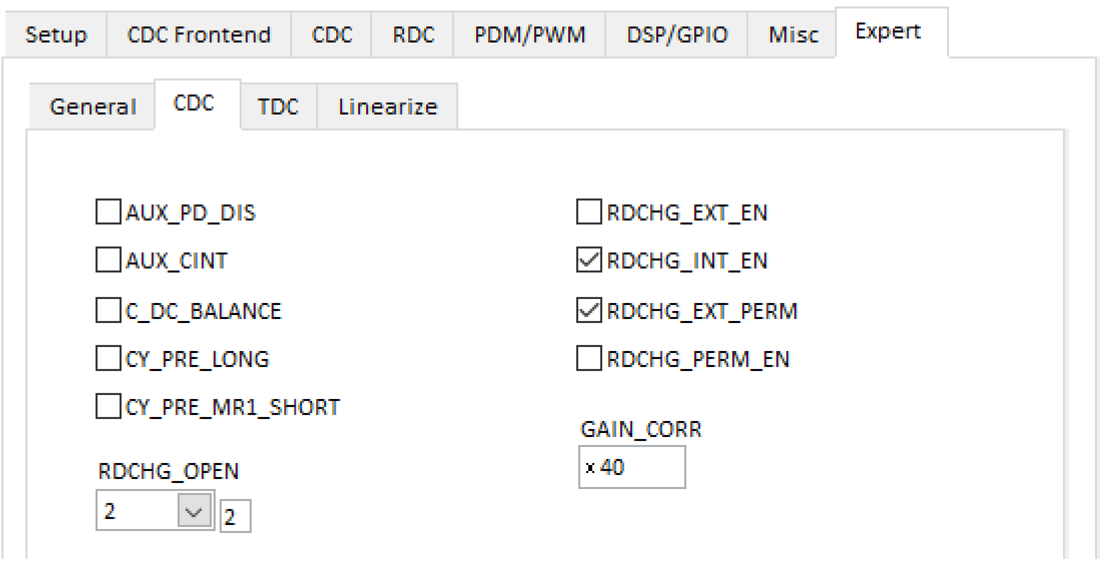

Figure 6: Expert Tab - CDC Tab

3 Evaluation of the Timing

3.1 Brief Summary

3.1.1 Capacitive-to-Digital Converter (CDC)

- Cycle Timing
  The basic period (t_{cycle}) that defines the cycle time can be derived from the low frequency oscillator or the high frequency oscillator. The pre-charge, full-charge and discharge times of a single cycle are defined in multiples of t_{cycle}.

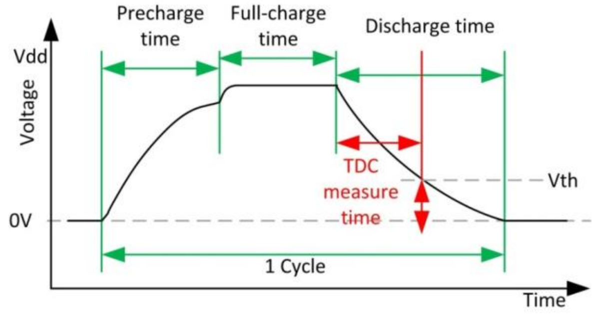

Figure 7: Single Cycle Timing

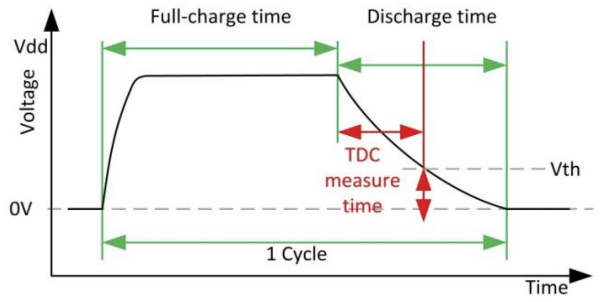

Figure 8: Single Cycle, Fast Charge

- Sequence
  The length of a sequence depends on the kind and number of sensors and the selected compensation methods.

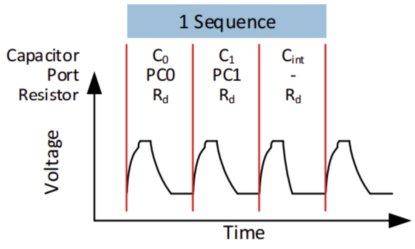

Figure 9: Sequence Grounded

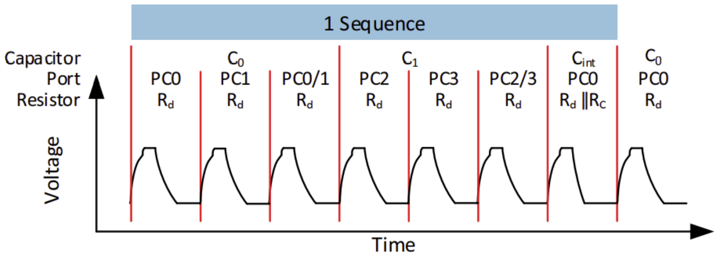

Figure 10: Sequence Floating

- Conversion
  The duration of a full conversion has a lower limit given by the number of fake measurements, the number of samples for averaging and eventually an inter-sequence delay. The Start of the next conversion depends on the selection of the measurement trigger.

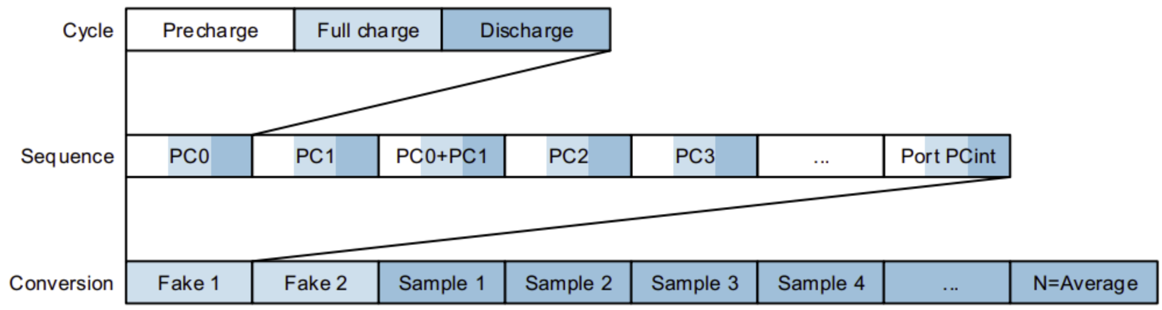

Figure 11: CDC Conversion

3.1.2 Resistance-to-Digital Converter (RDC)

- Cycle & Conversion
  In PCap04 the resistance measurement is running in three phases, like in capacitance measurement: Pre-charge – Full-charge – Discharge. The timing is based on the internal low-frequency oscillator (OLF). The duration of full and discharge phases can be 1 or 2 periods of this reference. The conversion starts with 2 or 8 fake measurements to improve the stability of data. For each single conversion the averaging can be selected with sample size 1, 4, 8 or 16.

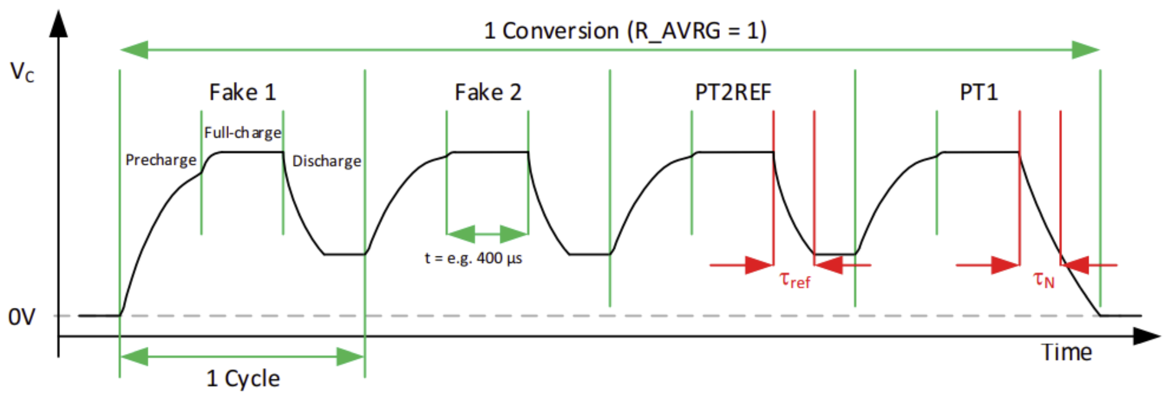

Figure 12: RDC Conversion (R_AVRG=1, reference and sensor, 2 fake measurements)

3.1.3 DSP

A 32-bit digital signal processor (DSP) in Harvard architecture was integrated to the PCap04. It is responsible for taking the information from the CDC and RDC measuring units, for processing the data and making them available to the user interface. Both, the CDC/RDC raw data as well as the data processed by the DSP are stored in the RAM.

The DSP is internally clocked at approximately 60 MHz and the needed post processing time depends on the used firmware (STANDARD-, LINARIZE- or customized firmware).

In order to reduce the post-processing time to a minimum, the RAW values only can be written to the read registers. This firmware is called MW2RES-firmware.

3.2 Choice the Reference

In these examples, STANDARD FW and default 'Standard' configuration is used. In case of using other capacitors, the configuration has to be adjusted. It is recommended to use reference capacity = sensor capacity.

3.3 Setup the Timing

For the demonstration of different discharge signals, an example with sensor = 10 pF and reference = 100 pF is used in this section. The sample size ('C_AVRG') is reduces to '3', internal 'Stray Compensation' and Conversion Mode (CDC->RDC->DSP->INT, see Figure 1) are used.

Note: It might be necessary to increase the 'Discharge time' to get rid of the possible error messages due to the probes. After removing the probes, adjust the discharge time once again.

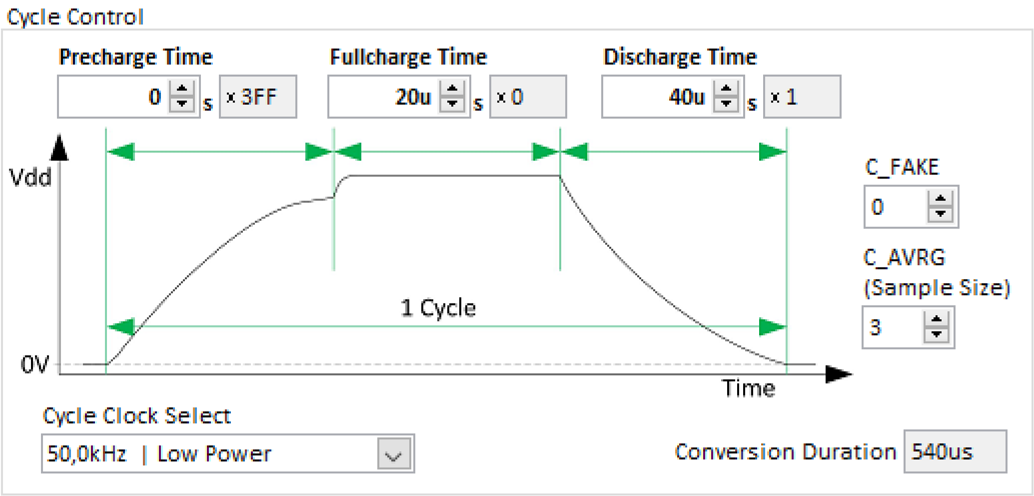

Figure 13: Used Cycle Control

Figure 14 shows a measurement based on that setting. The red cursors show a conversion time of 540 µs as configured. This timing is affected by the variation of the LF clock and can be tuned by means of parameter 'OLF_FTUNE'.

For grounded sensors, the sequence starts always with PC0 (reference) and then PC1 (sensor). Normally, internal compensation is activated. CDC sequence in detail (see Figure 9: Sequence Grounded) and due to the sample size (C_AVRG = 3), there are 3 sequences (C0, C1, Cint).

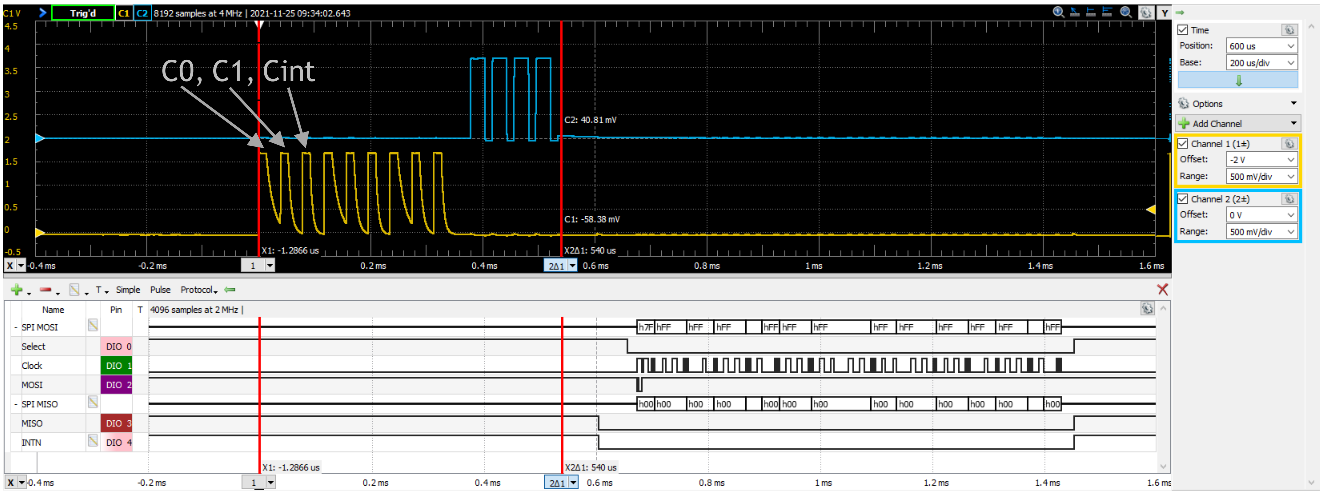

Figure 14: Measured CDC Sequence

Figure 15: Used LF Clock

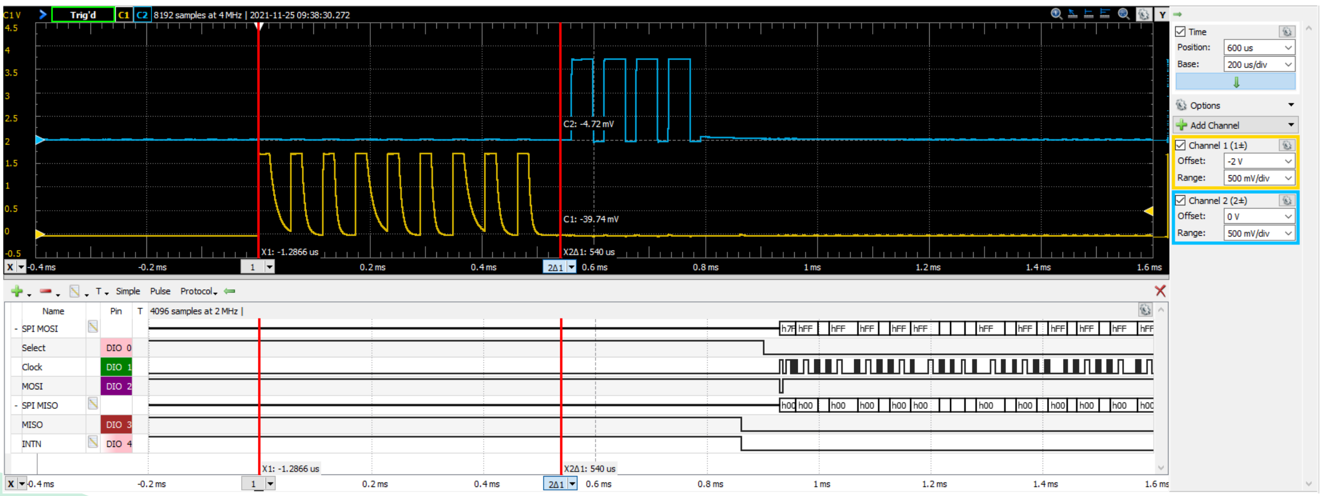

Figure 16: Adjusted CDC Sequence

4 Summary / Result

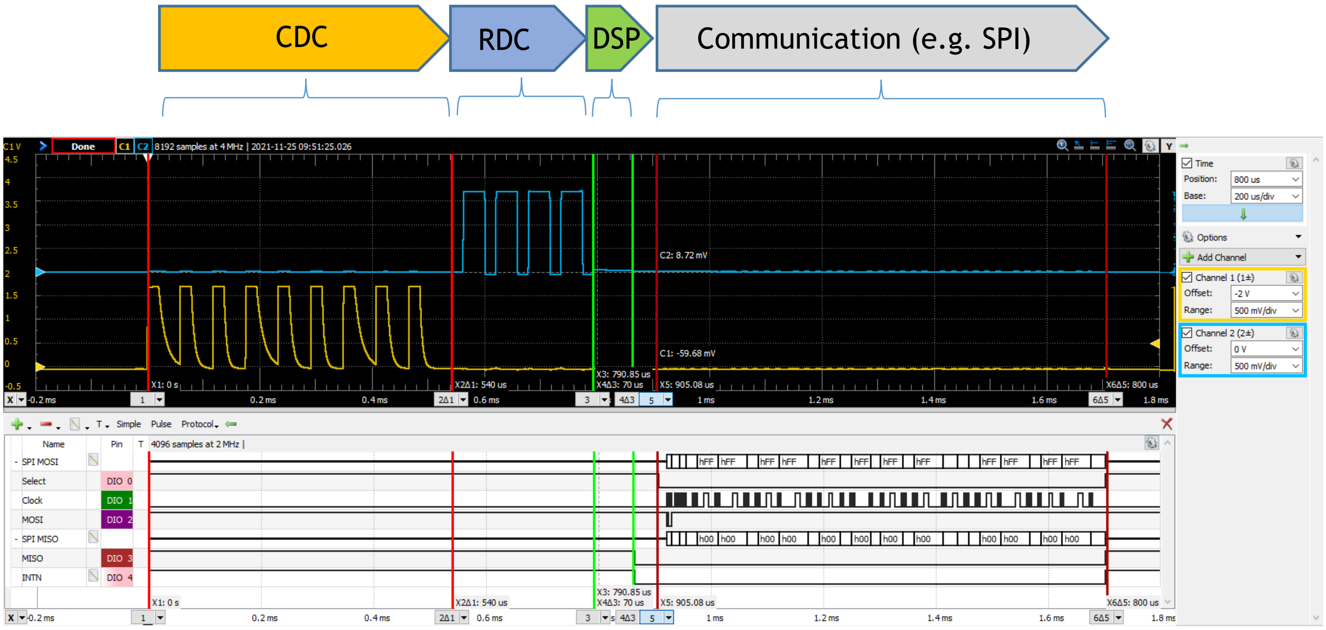

Figure 17: Complete Sequence (CDC->RDC->DSP->INT)

In this example the approximate timings are as follows:

- 540 µs (CDC)
- 230 µs (RDC, triggered by CDC)
- 70 µs (DSP, triggered by RDC)
- 1 ms (communication, e.g. SPI, triggered by DSP, which set the interrupt to low)

4.1 How to Increase the Update Rate

For a higher update rate it is necessary to reduce the CDC conversion duration, to switch off the RDC conversion and to optimize the communication frequency.

4.1.1 Communication Protocol

Optimization of communication protocol to a minimum can be done by increasing SPI frequency to the maximum specified frequency. For this maximum frequency a SPI bus termination is needed and recommended. In case of ignoring and not reading the status register to intercept possible readout error, the external microcontroller should perform a kind of plausibility check.

To read one result with SPI (20 MHz) it takes about 2.4 µs to send opcode (1 byte), address (1 byte) and to read Result (4 bytes).

$$6\,Byte * 8\,\frac{Bit}{Byte} * 50\,ns = 2.4\,\mu s$$

In this formula, the interbyte gap is ignored. Depending on the microcontroller, this timing can vary.

4.1.2 Conversion Duration

4.1.2.1.1 CDC Conversion

Now, following settings are used:

- Sensor = 1 pF
- Reference = internal (C_REF_INT = 1, C_REF_SEL = 0)
- Stray Compensation = ‘None’ (C_COMP_xxx = 0)
- Discharge Resistance Port 0..3 = ‘10k’ (RDCHG_INT_SEL0 = 3) For lower resistance, PCAUX can be used. But in this application note, PCAUX is used by scope.
- HF Clock

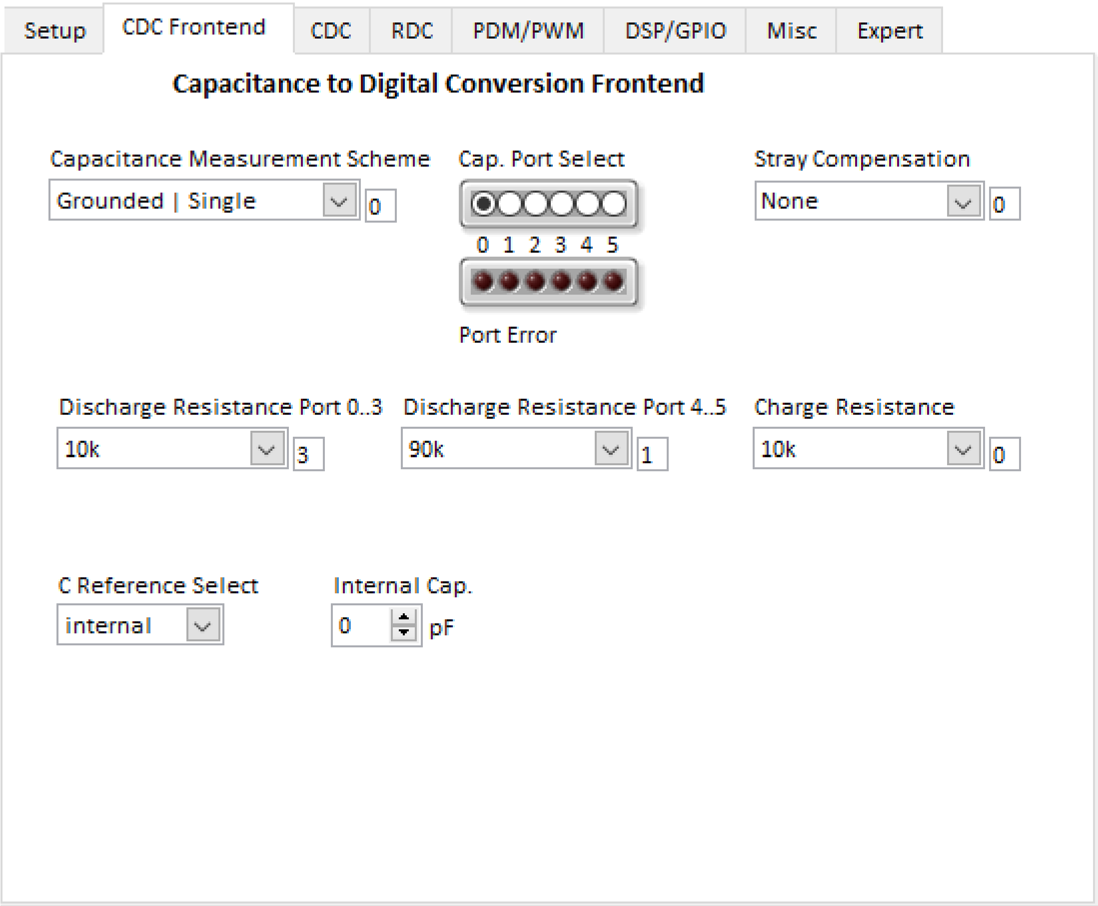

Figure 18: CDC Frontend Tab (reduced configuration)

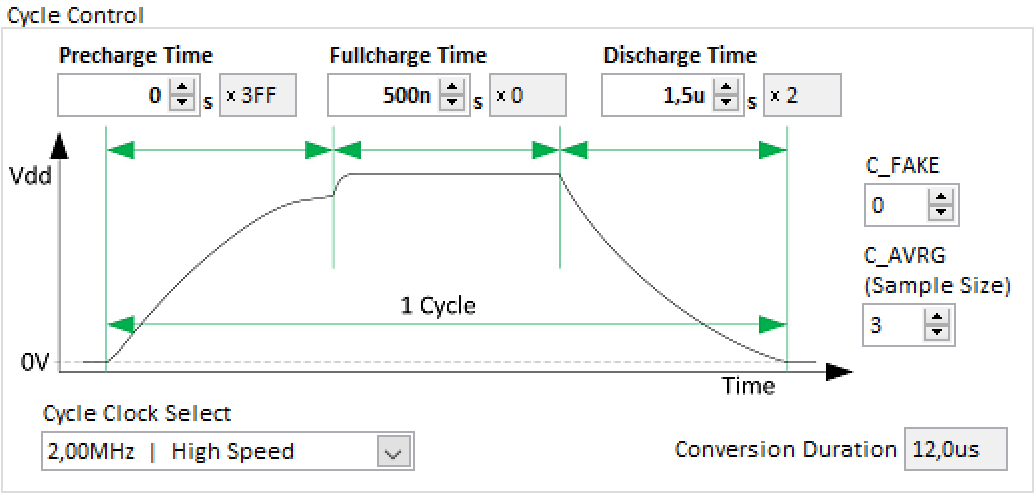

Figure 19: Cycle Control (reduced timing)

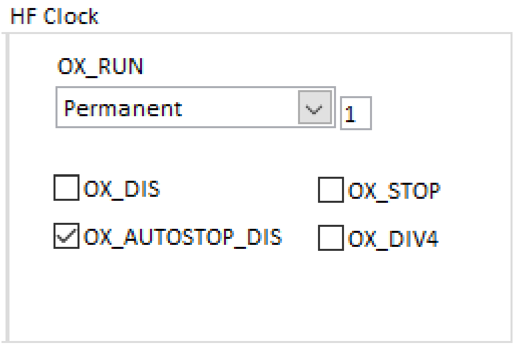

Figure 20: HF Clock (running permanent)

4.1.2.1.2 RDC Conversion

The CDC timer is based on the OLF. Therefore, the RDC conversion time can be reduced by changing LF Clock (OLF_TUNE, OLF_FTUNE). But for highest speed it should be switched OFF.

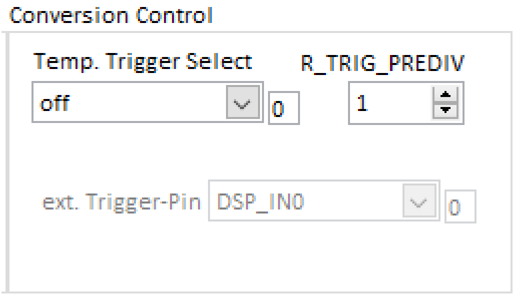

Figure 21: RDC - Conversion Control (trigger select = OFF)

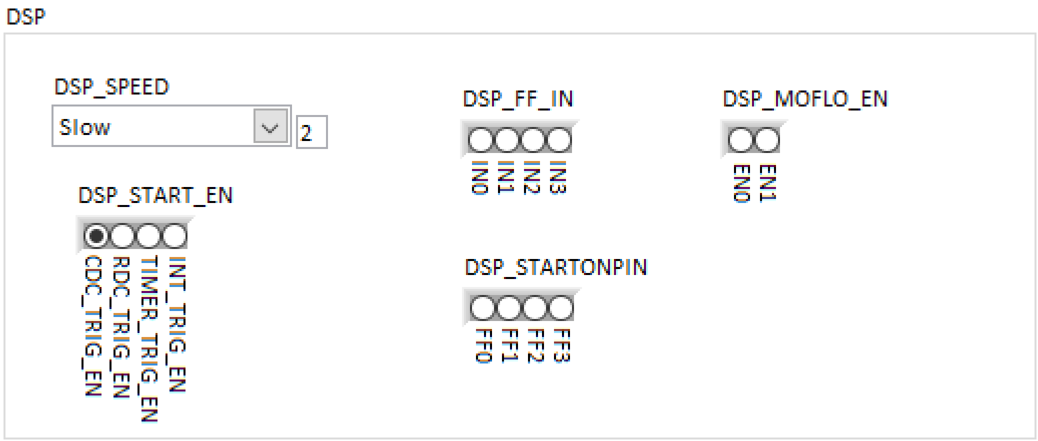

Figure 22: DSP (triggered by CDC)

4.1.2.1.3 DSP Execution Time

The configuration of DSP speed differs by ~15% from slowest to fastest speed.

Some DSP (approximate) timings:

- 50 µs, STANDARD FW (RDC = OFF, DSP_SPEED = ‘fastest’)
- 120 µs, LINEARIZE FW (needs RDC = ON, DSP_SPEED = fastest)
- 2 µs, MW2RES FW (RDC = OFF, DSP_SPEED = ‘fastest’)

4.2 Final Summary

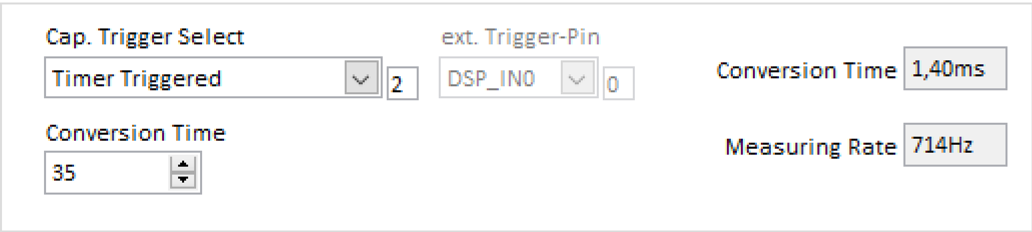

Figure 23: Conversion Control (for this example: Conversion Time using PICOPROG)

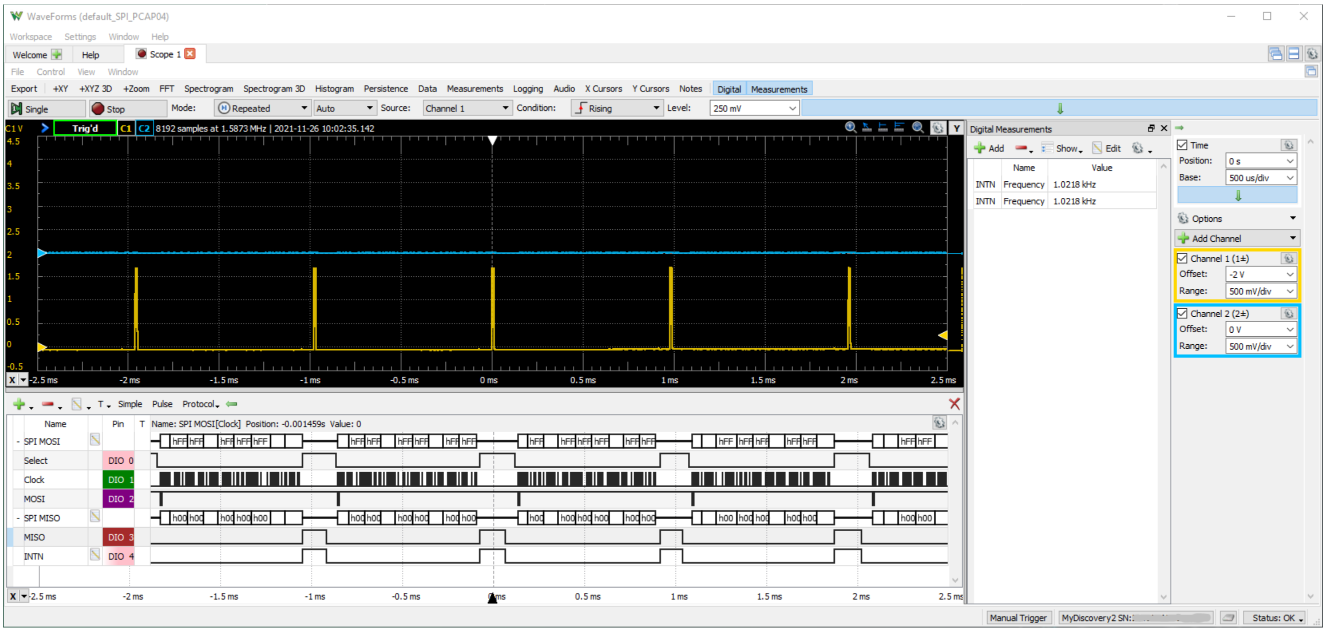

Figure 24: Scope (measuring sample rate)

The deviation of the configured ‘Measuring Rate’ = 714 Hz (Figure 23) from the measured measurement rate = 1 kHz (Figure 24) is due to the HF Clock and specified variation of PCap04 itself.

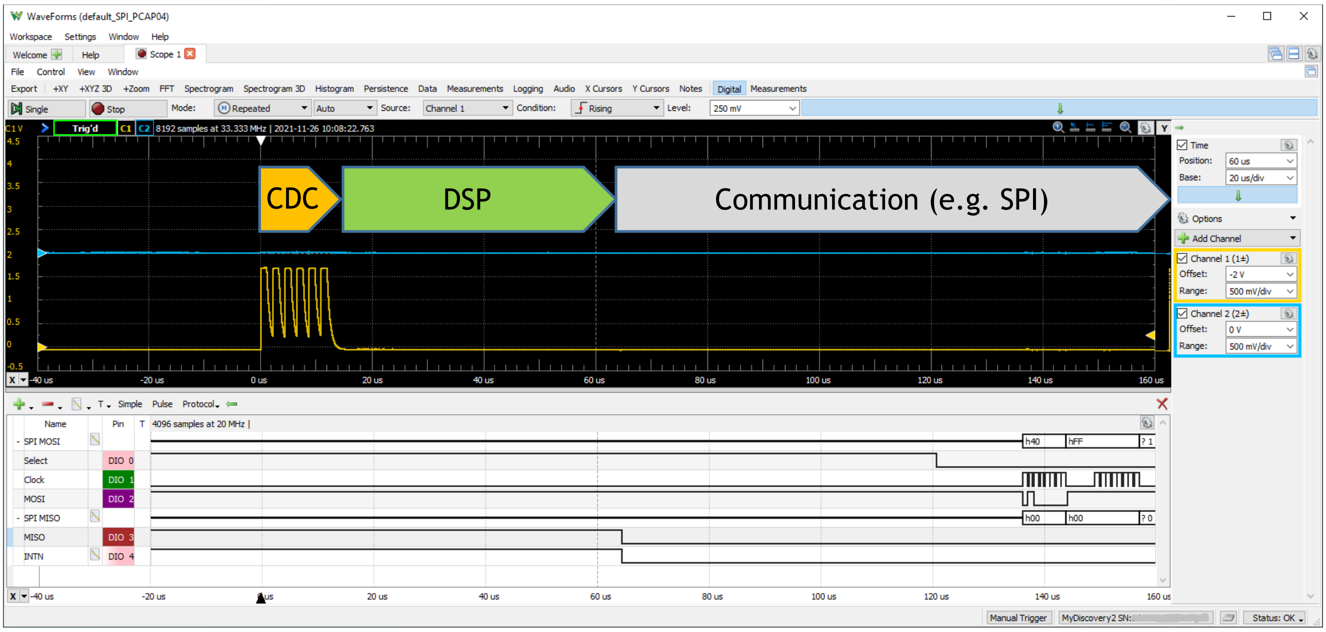

Figure 25: Scope, in details

The following example (again, with additional capacitive offset by probes) shows the case of using an external microcontroller with 20 MHz SPI Frequency and reading only one result. Further details are:

- 14 µs, CDC Conversion (C_AVRG = 3, …)
- 51 µs, DSP Execution Time (STANDARD FW, …)
- 3 µs, 20 MHz SPI Communication (reading one result, only)

Measurement rates < 15 kHz are possible without any great effort.

With further effort, such as:

- Using external discharge resistor to reduce the cycle time.
- Reducing average rate with considering the noise.
- Reducing DSP execution time.

It is possible to bring down the conversion time to 20 µs (< 50 kHz).

5 Copyrights & Disclaimer

6 Revision information

Table 1: Revision history

Revision	Date	Comment	Page
1	2021-12-01	First edition	All

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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