



# UFC23

## Ultrasonic Frontend

### UFC23 datasheet

Revision: 1

Release Date: 2026-05-12

Document Status: Preliminary

UFC23 is a frontend for ultrasonic flow measurements in water, heat and gas meters. It uses an high-performance front-end capable of driving two transducers and processing the received signal to extract the time of flight (TOF) information with high precision and offset stability.

An highly programmable amplifier up to 60 dB (gas) and 20dB (water) allows handling weak receive amplitudes. A fire burst generator generates bursts up to 4.4 MHz, based on up to 20 MHz reference. A split burst feature supports correction of phase jumps. Besides the 3.3V single-ended drivers the UFC23 offers full-bridge drivers for increased voltage across the transducer. The combination of full-bridge, higher gain, higher bandwidth and frequency adjustment make it suitable for gas meter applications.

A 160-words RAM allows access to all time data but also accumulation of data (batch mode) and reduced wake-up of external  $\mu\text{C}$ .

With  $1\mu\text{A}$  standby current and low operation current it is optimized for battery-operated systems.

## Key Benefits

- High precision
- Low power
- Proven technology
- System cost reduction

## Key Features

- 3.3V Single-ended or full-bridge driver for transducers
- Fire frequency generator up to 4.4 MHz, based on reference up to 20 MHz
- PGA with increased gain and increased bandwidth
- Low noise (E.g. 35 ps single shot with DN15) and excellent offset-stability (E.g.  $\pm 7$  ps with 100 samples average at  $25^\circ\text{C}$ )
- Combination full-bridge, higher gain, higher bandwidth and frequency adjustment make it suitable for gas meter applications

- Improved current management to reduce standby current (cycle timer off)  $I_{\text{stby}} \sim 0.8 \mu\text{A} @ 25^\circ\text{C}$
- Increased RAM (160 words) for access to all time data but also for accumulation of data and reduced wake-up of external  $\mu\text{C}$

## Applications

- Smart water & heat meters
- Smart gas meters
- Water heaters
- Pump control
- Smart faucets & showers

## Properties

- Supply voltage 2.5 to 3.6 V
- Temperature range  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- QFN32 package

## Content Guide

|   |           |   |           |
|---|-----------|---|-----------|
| <b>Content Guide</b> .....                      | <b>3</b>  | <b>8 RAM Content</b> .....                      | <b>44</b> |
| <b>1 Block Diagram</b> .....                    | <b>4</b>  | 8.1 Single Cycle Mode .....                     | 44        |
| <b>2 Pin Assignment</b> .....                   | <b>5</b>  | 8.2 USM Bundle .....                            | 45        |
| <b>3 Absolute Maximum Ratings</b> .....         | <b>7</b>  | 8.3 Batch Cycle Mode .....                      | 46        |
| <b>4 Recommended Operating Conditions</b> ..... | <b>7</b>  | 8.4 Frontend Error and Status Flags .....       | 47        |
| <b>5 Electrical Characteristics</b> .....       | <b>8</b>  | 8.5 Temperature results .....                   | 48        |
| <b>6 Detailed Description</b> .....             | <b>14</b> | 8.6 Result & Status Format within Bundle        | 49        |
| 6.1 Time of flight Measuring Principle ...      | 14        | <b>9 Configuration Registers</b> .....          | <b>51</b> |
| 6.2 Measurement Operations .....                | 14        | 9.1 Register overview .....                     | 51        |
| 6.3 Fire Buffers, Receivers & Burst             |           | 9.2 Detailed register description .....         | 52        |
| Generation .....                                | 17        | 9.3 Reference Configuration .....               | 66        |
| 6.4 PGA .....                                   | 19        | <b>10 Application Information</b> .....         | <b>67</b> |
| 6.5 Time-of-Flight (ToF) Measurement ..         | 23        | 10.1 Schematic .....                            | 67        |
| 6.6 Amplitude Measurement .....                 | 27        | 10.2 Code Examples .....                        | 68        |
| 6.7 Sub-Tasks execution .....                   | 28        | <b>11 Soldering information</b> .....           | <b>69</b> |
| 6.8 Temperature Measurement .....               | 29        | <b>12 Package drawings &amp; markings</b> ..... | <b>70</b> |
| 6.9 TOF Error Handling .....                    | 31        | <b>13 Ordering information</b> .....            | <b>72</b> |
| 6.10 Batch mode .....                           | 32        | <b>14 RoHS Compliance &amp; ScioSense Green</b> |           |
| 6.11 Interrupts and flags .....                 | 32        | <b>Statement</b> .....                          | <b>73</b> |
| <b>7 Host communication</b> .....               | <b>36</b> | <b>15 Copyrights &amp; Disclaimer</b> .....     | <b>73</b> |
| 7.1 Task Execution .....                        | 37        | <b>16 Document status</b> .....                 | <b>74</b> |
| 7.2 Flag Register Read .....                    | 41        | <b>17 Revision information</b> .....            | <b>74</b> |
| 7.3 Random Area Access .....                    | 42        |   |           |

# 1 Block Diagram

The functional blocks of this device are shown below.

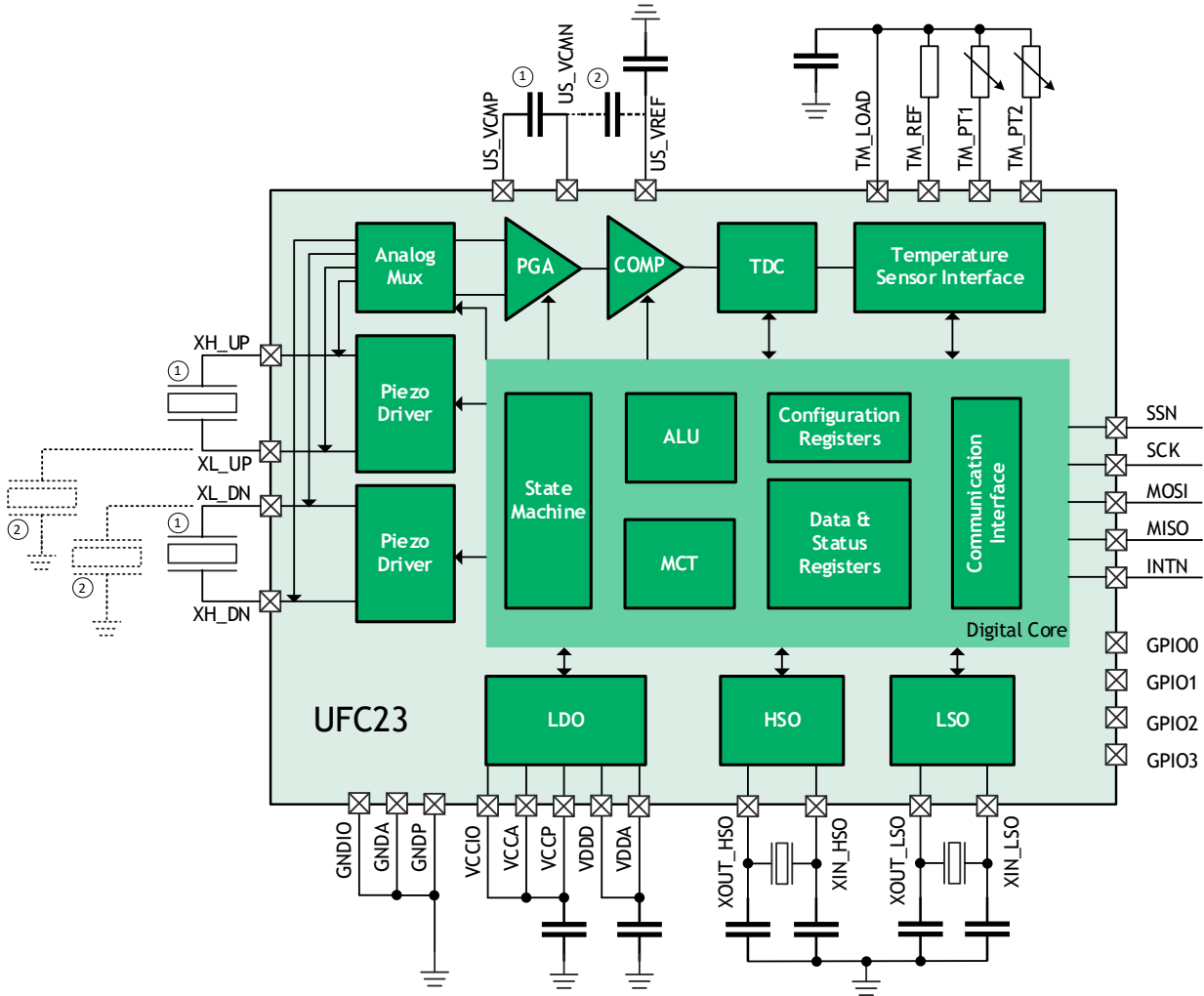


Figure 1: Functional Blocks

<sup>1</sup> Differential connection of sensors  
<sup>2</sup> Single-ended connection of sensors

## 2 Pin Assignment

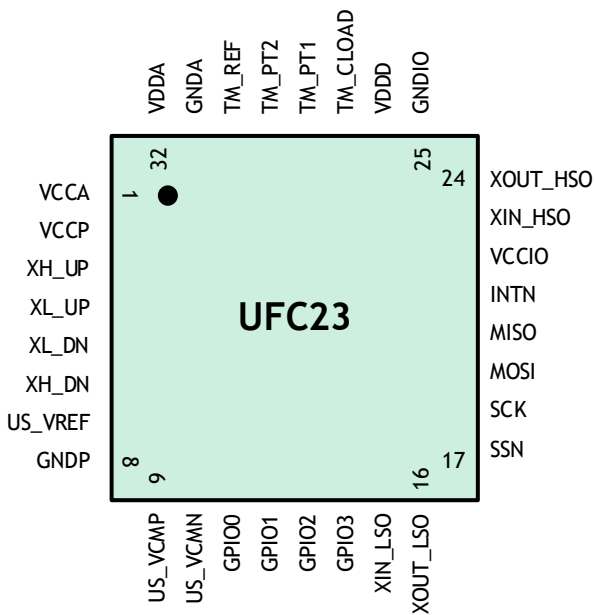


Figure 2: Pin diagram

Table 1: Pin description

| Pins | Pin Name | System    | Pin Type       | Description  |
|------|----------|-----------|----------------|--|
| 1    | VCCA     | Gas/Water | Supply         | Battery Voltage - Analog Block                     |
| 2    | VCCP     | Gas/Water | Supply         | Battery Voltage – US driver                        |
| 3    | XH_UP    | Gas       | Analog IO      | US Transceiver - transducer up positive terminal   |
| 4    | XL_UP    | Gas/Water | Analog IO      | US Transceiver - transducer up negative terminal   |
| 5    | XL_DN    | Gas/Water | Analog IO      | US Transceiver - transducer down positive terminal |
| 6    | XH_DN    | Gas       | Analog IO      | US Transceiver - transducer down negative terminal |
| 7    | US_VREF  | Gas/Water | Analog IO      | Ultrasonic Reference Voltage for Receive Path      |
| 8    | GNDP     | Gas/Water | Ground         | Ground – US driver                                 |
| 9    | US_VCMP  | Gas/Water | Analog IO      | Ultrasonic PGA Output Cap                          |
| 10   | US_VCMN  | Gas/Water | Analog IO      | Ultrasonic PGA Output Cap                          |
| 11   | GPIO0    | Gas/Water | DIO/AIO        | General Purpose IO 0                               |
| 12   | GPIO1    | Gas/Water | DIO/AIO        | General Purpose IO 1                               |
| 13   | GPIO2    | Gas/Water | DIO/AIO        | General Purpose IO 2                               |
| 14   | GPIO3    | Gas/Water | DIO/AIO        | General Purpose IO 3                               |
| 15   | XIN_LSO  | Gas/Water | Analog IO      | Low Speed Oscillator - Input                       |
| 16   | XOUT_LSO | Gas/Water | Analog IO      | Low Speed Oscillator - Output                      |
| 17   | SSN      | Gas/Water | Digital input  | SPI: Sub Select (low active)                       |
| 18   | SCK      | Gas/Water | Digital input  | SPI: Serial Clock                                  |
| 19   | MOSI     | Gas/Water | Digital input  | SPI: Main Out, Sub In                              |
| 20   | MISO     | Gas/Water | Digital Output | SPI: Main In , Sub Out                             |

|    |          |           |                |  |
|----|----------|-----------|----------------|--|
| 21 | INTN     | Gas/Water | Digital Output | Interrupt (low active)                       |
| 22 | VCCIO    | Gas/Water | Supply         | Battery Voltage – Periphery                  |
| 23 | XIN_HSO  | Gas/Water | Analog IO      | High Speed Oscillator - Input                |
| 24 | XOUT_HSO | Gas/Water | Analog IO      | High Speed Oscillator - Output               |
| 25 | GNDIO    | Gas/Water | Ground         | Ground – Periphery                           |
| 26 | VDDD     | Gas/Water | Analog IO      | Digital Low Voltage Supply                   |
| 27 | TM_CLOAD | Gas/Water | Analog IO      | Temperature Measurement: Discharge Capacitor |
| 28 | TM_PT1   | Gas/Water | Analog IO      | Temperature Measurement, first PT sensor     |
| 29 | TM_PT2   | Gas/Water | Analog IO      | Temperature Measurement: second PT sensor    |
| 30 | TM_REF   | Gas/Water | Analog IO      | Temperature Measurement: Reference Resistor  |
| 31 | GNDA     | Gas/Water | Ground         | Analog Low Voltage Ground                    |
| 32 | VDDA     | Gas/Water | Analog IO      | Analog Low Voltage Supply                    |

### 3 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only.

Table 2: Absolute Maximum Ratings

| Symbol             | Parameter                                  | Comments   | Min                 | Max     | Units |
|--------------------|--|--|---------------------|---------|-------|
| V <sub>CC</sub>    | Supply Voltage                             | Voltages relative to GNDIO<br>Pins VCCA, VCCP, VCCIO | -0.3                | 4       | V     |
| V <sub>OTH</sub>   | All other Pins Voltage                     | Voltages relative to GNDIO,<br>not to exceed 4.0V    | -0.3                | VCC+0.3 | V     |
| V <sub>TMI</sub>   | DC voltage at TM_PT1, TM_PT2<br>and TM_REF | Voltages relative to GNDIO                           | -0.3                | 4       | V     |
| I <sub>SCR</sub>   | Input Current (latch-up immunity)          | AEC-Q100-004   | -100                | 100     | mA    |
| ESD <sub>HBM</sub> | Electrostatic Discharge HBM                | JS-001-2014  | ± 2000 <sup>3</sup> |         | V     |
| ESD <sub>CDM</sub> | Electrostatic Discharge CDM                | JS-002-2014  | ± 500               |         | V     |
| MSL                | Moisture Sensitivity Level                 | Unlimited floor lifetime                             | 3                   |         |       |
| T <sub>BODY</sub>  | Max. Package Body Temperature              | IPC/JEDEC J-STD-020                                  |                     | 260     | °C    |
| T <sub>STRG</sub>  | Storage Temperature                        |  | -55                 | 150     | °C    |

### 4 Recommended Operating Conditions

Recommended operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Table 3: Recommended operation conditions

| Symbol                            | Parameter                         | Conditions                         | Min       | Typ | Max       | Unit |
|-----------------------------------|-----------------------------------|------------------------------------|-----------|-----|-----------|------|
| <b>Power Supply</b>               |                                   |                                    |           |     |           |      |
| V <sub>CC</sub>                   | DC supply voltage                 | Pins VCCA, VCCP,<br>VCCIO          | 2.5       | 3.3 | 3.6       | V    |
| V <sub>DD</sub>                   | Internal LDO output               | Pins VDD, VDDA                     | 1.62      | 1.8 | 1.98      | V    |
| <b>Temperature</b>                |                                   |                                    |           |     |           |      |
| T <sub>AMB</sub>                  | Operating free air<br>temperature |                                    | -40       |     | 85        | °C   |
| <b>Digital Inputs and Outputs</b> |                                   |                                    |           |     |           |      |
| V <sub>OH</sub>                   | High-level output voltage         | MISO, INTN I <sub>oh</sub> = 16 mA | 0.8 * VCC |     |           | V    |
| V <sub>OL</sub>                   | Low-level output voltage          | GPIOx I <sub>oh</sub> = 4 mA       |           |     | 0.4       | V    |
| V <sub>IH</sub>                   | High-level input voltage          |                                    | 0.7 * VCC |     |           | V    |
| V <sub>IL</sub>                   | Low-level input voltage           |                                    |           |     | 0.3 * VCC | V    |
| V <sub>IH_LL</sub>                | High-level input voltage          | Low leakage                        | 0.8 * VCC |     |           | V    |

<sup>3</sup> For B- and C-samples this is not true for pin 1. True for production release.

|                             |                         |             |   |   |           |     |
|-----------------------------|-------------------------|-------------|---|---|-----------|-----|
| V <sub>IL_LL</sub>          | Low-level input voltage | Low leakage |   |   | 0.2 * VCC | V   |
| Oscillator                  |                         |             |   |   |           |     |
| F <sub>H<sub>SO</sub></sub> | Oscillator Frequency    |             | 4 | 8 | 20        | MHz |

## 5 Electrical Characteristics

(VCC = +2.5V to +3.6V, T<sub>AMB</sub> = -40°C to +85°C, VDD = +1.62V to +1.98V, unless otherwise noted. Typical values are at VCC = 3.3V, VDD=1.8V and T<sub>AMB</sub> = +25°C.)

Table 4: Electrical characteristics

| Symbol               | Parameter                           | S <sup>4</sup> | Conditions  | Min | Typ         | Max | Unit |
|----------------------|-------------------------------------|----------------|---|-----|-------------|-----|------|
| I <sub>CC</sub>      | Average Supply Current <sup>5</sup> | W              | without PGA<br>2 Hz<br>8 Hz   |     | 2.3<br>6.6  |     | μA   |
| I <sub>CC</sub>      | Average Supply Current <sup>5</sup> | W              | with PGA<br>gain 3<br>2 Hz<br>8 Hz  |     | 2.6<br>7.5  |     | μA   |
| I <sub>CC</sub>      | Average Supply Current <sup>5</sup> | G              | with PGA<br>gain 31 * 4<br>2 Hz<br>8 Hz   |     | 5.5<br>19.1 |     | μA   |
| I <sub>CC_STBY</sub> | Standby Current                     |                | No measurement, measure cycle timer off, T <sub>AMB</sub> = +25°C   |     | 0.8         |     | μA   |
| D <sub>TOF_ACC</sub> | Time of Flight Difference Accuracy  | W              | Standard deviation single-shot over 500 measurements with typ. DN15 <sup>6</sup> sensor<br>Stability with average 128 |     | 35<br>±7    |     | ps   |
| D <sub>TOF_ACC</sub> | Time of Flight Difference Accuracy  | G              | Standard deviation of 500 measurements, 500kHz transducers  |     | 500         |     | ps   |
| D <sub>TOF_TD</sub>  | Differential TOF temperature drift  | W              | Drift over temperature of the average of 500 measurements with PAL, 5°C to 50°C                                       |     | 10          |     | ps   |
| D <sub>TOF_TD</sub>  | Differential TOF temperature drift  | G              | Drift over temperature of the average of 500 measurements with PAL, -40°C to 85°C                                     |     | 30          |     | ps   |
| F <sub>LSO</sub>     | Low Speed Oscillator Frequency      |                | ± 30 ppm over temperature   |     | 32.768      |     | kHz  |

<sup>4</sup> System application: 3 V, 16 MHz ref., W = water meters (70 μs ToF), G = gas meters (220 μs ToF)

<sup>5</sup> Measurement only, without communication

<sup>6</sup> E.g. Ceramtec DN15 with 2 MHz transducers

| Symbol                      | Parameter                          | S <sup>4</sup> | Conditions   | Min                   | Typ   | Max                       | Unit |
|-----------------------------|------------------------------------|----------------|--|-----------------------|---|---------------------------|------|
| F <sub>H<sub>SO</sub></sub> | High Speed Oscillator Frequency    | W<br>G         | ± 0.5 %  |                       | 4<br>8<br>12<br>16<br>20                      |                           | MHz  |
| TOF <sub>RNG</sub>          | Ultrasonic Time Of Flight Range    | G              | Up to 16 MHz F <sub>H<sub>SO</sub></sub>                             | 30                    |   | 8000                      | µs   |
| TOF <sub>RNG</sub>          | Ultrasonic Time Of Flight Range    | W              |  | 30                    |   | 1000                      | µs   |
| F <sub>US_FIRE</sub>        | Ultrasonic Fire Frequency          | G              |  | 180                   |   | 550                       | kHz  |
| F <sub>US_FIRE</sub>        | Ultrasonic Fire Frequency          | W              | F <sub>H<sub>SO</sub></sub> ≥ 4 * F <sub>US_FIRE</sub>               | 0.8                   |   | 4.4                       | MHz  |
| F <sub>SPLIT_RNG</sub>      | Split burst range                  |                | T <sub>US_F</sub> = 1 / F <sub>US_FIRE</sub>                         | T <sub>US_F</sub> / 4 |   | 8 * T <sub>US_F</sub> / 4 |      |
| F <sub>SPLIT_RES</sub>      | Split burst resolution             |                | T <sub>US_F</sub> = 1 / F <sub>US_FIRE</sub>                         |                       | T <sub>US_F</sub> / 4                         |                           |      |
| AM <sub>ACC</sub>           | Amplitude Measurement Accuracy     |                | 200mV input signal amplitude   | -25                   |   | 25                        | mV   |
| TOF <sub>LSB</sub>          | TOF result resolution              |                | 1 LSB, T <sub>H<sub>SO</sub></sub> = 1 / F <sub>H<sub>SO</sub></sub> |                       | T <sub>H<sub>SO</sub></sub> / 2 <sup>16</sup> |                           |      |
| PW <sub>LSB</sub>           | PW result resolution               |                | 1 LSB, T <sub>H<sub>SO</sub></sub> = 1 / F <sub>H<sub>SO</sub></sub> |                       | T <sub>H<sub>SO</sub></sub> / 2 <sup>10</sup> |                           |      |
| R <sub>M</sub>              | Internal Matching Resistance Range | W              | Single ended   | 32                    |   | 838                       | Ω    |
| R <sub>M</sub>              | Internal Matching Resistance Range | G              | Differential   | 64                    |   | 1676                      | Ω    |
| R <sub>MSTEP</sub>          | Internal Matching Resistance Step  |                | Single ended differential  |                       | 26<br>52                                      |                           | Ω    |
| VIN <sub>PGA</sub>          | Receiver Input Amplitude           | W              | V <sub>REF</sub> = 700mV   | 25                    |   | 500                       | mV   |
| VIN <sub>PGA</sub>          | Receiver Input Amplitude           | G              | V <sub>REF</sub> = 700mV   | tbd                   |   | 250                       | mV   |
| FHL <sub>RNG</sub>          | First Hit Level Detection Range    |                |  | 5                     |   | 200                       | mV   |

| Symbol                            | Parameter  | S <sup>4</sup> | Conditions  | Min            | Typ                            | Max   | Unit |
|-----------------------------------|--|----------------|---|----------------|--------------------------------|-------|------|
| SAR <sub>LSB</sub>                | SAR10 ADC LSB  |                | 1.4V / 1024   |                | 1.37                           |       | mV   |
| MW <sub>RES</sub>                 | Delay mask window resolution                             |                | High resolution mask window<br>$F_{H_{SO}} \geq 4 * F_{US\_FIRE}$                   |                | 1/ F <sub>H<sub>SO</sub></sub> |       | ns   |
| VM <sub>RNG</sub>                 | V <sub>CC</sub> measurement range                        |                | s   | 2.35           |                                | 3.725 | V    |
| VM <sub>STEP_V<sub>CC</sub></sub> | V <sub>CC</sub> measurement resolution                   |                | 1 LSB   |                | 2.93*<br>SAR <sub>LSB</sub>    |       | mV   |
| VM <sub>STEP_V<sub>DD</sub></sub> | V <sub>DD</sub> measurement resolution                   |                | 1 LSB   |                | 1.97*<br>SAR <sub>LSB</sub>    |       | mV   |
| VM <sub>ACC</sub>                 | V <sub>CC</sub> and V <sub>DD</sub> measurement accuracy |                |   | -5             |                                | 5     | %    |
| N <sub>HITS</sub>                 | Single TOF storage                                       |                | In up/down direction  | 1              |                                | 61    |      |
| N <sub>TXPLS</sub>                | Transmit Burst Fire Pulses                               |                |   | 4 <sup>7</sup> |                                | 63    |      |
| f <sub>LDOrefresh</sub>           | Refresh rate for VDD external capacity                   |                | C_VDD:<br>10...100 uF<br><br>Refresh rate shall be set in order to have VDD > 1.62V | 0.5            |                                | 64    | Hz   |
| H <sub>SO</sub> STUP              | HFO settling time for ± 0.5 %                            |                | Depending on external resonator nominal frequency                                   |                |                                | 300   | µs   |

<sup>7</sup> Can be 1 for f<sub>H<sub>SO</sub></sub> = 8 MHz and f<sub>Fire</sub> = 1 MHz, or 1 for f<sub>H<sub>SO</sub></sub> = 16 MHz, f<sub>Fire</sub> = 1 MHz and C\_FEP\_4M\_CLK\_DIV = 2

### 5.1.1 Temperature Interface

(VCC = +2.5V to +3.6V, T<sub>AMB</sub> = -40°C to +85°C, VDD = +1.62V to +1.98V, unless otherwise noted. Typical values are at VCC = 3.3V, VDD=1.8V and T<sub>AMB</sub> = +25°C.).

2-wire measurement with compensation of R<sub>ds(on)</sub> and gain (Schmitt-Trigger). All values measured @ C<sub>Load</sub> = 100 nF for PT1000 and 200 nF for PT500 (COG-type)

Table 5: Temperature interface characteristics

| Symbol              | Parameter                  | Conditions                               | Min | Typ  | Max | Unit  |
|---------------------|----------------------------|--|-----|------|-----|-------|
| TM <sub>RES</sub>   | Resolution RMS             |  |     | 17   |     | Bit   |
| G <sub>VCCDFT</sub> | Gain-Drift vs. VCC         | Compared to an ideal gain of 1.0         |     | 0.01 |     | %/V   |
| G <sub>TDFT</sub>   | Gain-Drift vs. Temperature | Compared to an ideal gain of 1.0, PT500  |     | 4    |     | ppm/K |
| G <sub>TDFT</sub>   | Gain-Drift vs. Temperature | Compared to an ideal gain of 1.0, PT1000 |     | 2    |     | ppm/K |
| TM <sub>ZOFF</sub>  | Initial Zero Offset        | PT500                                    |     | 40   |     | mK    |
| TM <sub>ZOFF</sub>  | Initial Zero Offset        | PT1000                                   |     | 20   |     | mK    |

### 5.1.2 Power On Timings

(VCC = +2.5V to +3.6V, T<sub>AMB</sub> = -40°C to +85°C, VDD = +1.62V to +1.98V, unless otherwise noted. Typical values are at VCC = 3.3V, VDD=1.8V and T<sub>AMB</sub> = +25°C.)

Table 6: Power-on Timings

| Symbol               | Parameter                               | Conditions   | Min | Typ | Max                         | Unit |
|----------------------|---|--|-----|-----|-----------------------------|------|
| t <sub>VDDSTBL</sub> | Stable Time VDD (after power on of VCC) | T <sub>A</sub> = 25 °C, CVDD18 = 100uF                   |     |     | 10                          | ms   |
| t <sub>LSOSTUP</sub> | Startup Time Low Speed Oscillator       | T <sub>A</sub> = 25 °C, Oscillation start after power on |     | 200 |                             | ms   |
| t <sub>RCRLS</sub>   | Release time for remote communication   |  |     |     | t <sub>LSOSTUP</sub> + 32   | ms   |
| t <sub>MMRLS</sub>   | Release time for measure mode           |  |     |     | t <sub>LSOSTUP</sub> + 1000 | ms   |

### 5.1.3 Measurement Timings

(VCC = +2.5V to +3.6V, T<sub>AMB</sub> = -40°C to +85°C, VDD = +1.62V to +1.98V, unless otherwise noted. Typical values are at VCC = 3.3V, VDD=1.8V and T<sub>AMB</sub> = +25°C.)

Table 7: Measurement Timings

| Symbol                 | Parameter   | Conditions                           | Min                           | Typ | Max                            | Unit |
|------------------------|---|--------------------------------------|-------------------------------|-----|--------------------------------|------|
| t <sub>MSR_CYCLE</sub> | Measure Rate Cycle Time                             | 1 LSB: 0.9765625 ms                  | 10                            |     | 3999                           | ms   |
| t <sub>MSR_US_WM</sub> | Ultrasonic Measure Rate for Water Meter Application | No temperature measurement activated | 10                            |     | 3999                           | ms   |
| t <sub>MSR_US_HM</sub> | Ultrasonic Measure Rate for Heat Meter Application  | Temperature measurement activated    | 50                            |     | 3999                           | ms   |
| t <sub>MSR_TM</sub>    | Temperature Measurement Period                      |                                      | 0.05                          | 30  |                                | sec  |
| t <sub>MSR_HCC</sub>   | High Speed Clock Calibration Period                 |                                      | 1 *<br>t <sub>MSR_CYCLE</sub> |     | 64 *<br>t <sub>MSR_CYCLE</sub> | ms   |
| t <sub>MSR_ZCC</sub>   | Zero Cross Calibration Period                       |                                      | 1 *<br>t <sub>MSR_CYCLE</sub> |     | 64 *<br>t <sub>MSR_CYCLE</sub> | ms   |

### 5.1.4 SPI Timings

(VCC = +2.5V to +3.6V, T<sub>AMB</sub> = -40°C to +85°C, VDD = +1.62V to +1.98V, unless otherwise noted. Typical values are at VCC = 3.3V, VDD=1.8V and T<sub>AMB</sub> = +25°C.)

Table 8: SPI interface characteristics

| Symbol             | Parameter                             | Conditions | Min                     | Typ | Max | Unit |
|--------------------|---------------------------------------|------------|-------------------------|-----|-----|------|
| f <sub>SCK</sub>   | Serial clock frequency                |            |                         |     | 20  | MHz  |
| t <sub>SCK</sub>   | Serial clock time period              |            | 50                      |     |     | ns   |
| t <sub>pwh</sub>   | Serial clock, pulse width high        |            | 0.45 * t <sub>SCK</sub> |     |     | ns   |
| t <sub>pwl</sub>   | Serial clock, pulse width low         |            | 0.45 * t <sub>SCK</sub> |     |     | ns   |
| t <sub>sussn</sub> | SSN enable to valid latch clock       |            | 0.5 * t <sub>SCK</sub>  |     |     | ns   |
| t <sub>hssn</sub>  | SSN hold time after SCK falling       |            | 0.5 * t <sub>SCK</sub>  |     |     | ns   |
| t <sub>pwssn</sub> | SSN pulse width between two cycles    |            | t <sub>SCK</sub>        |     |     | ns   |
| t <sub>sud</sub>   | Data set-up time prior to SCK falling |            | 5                       |     |     | ns   |

| Symbol   | Parameter                         | Conditions | Min | Typ | Max | Unit |
|----------|-----------------------------------|------------|-----|-----|-----|------|
| $t_{hd}$ | Data hold time before SCK falling |            | 5   |     |     | ns   |
| $t_{vd}$ | Data valid after SCK rising       |            |     |     | 25  | ns   |

Figure 3:SPI Write

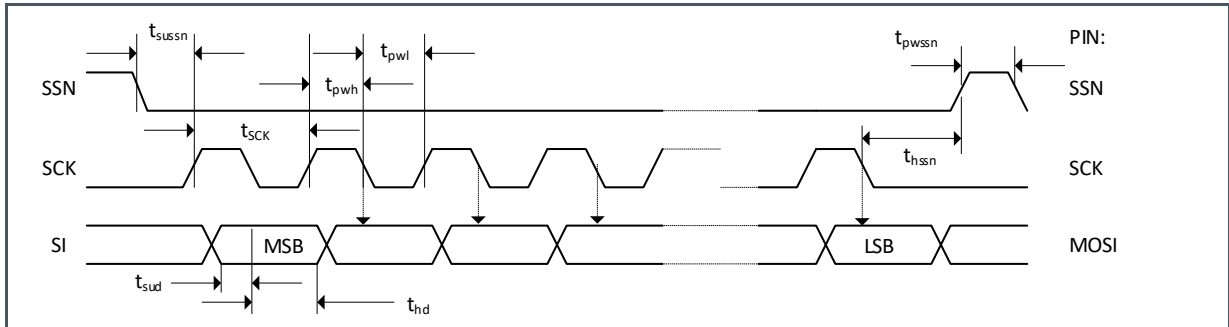
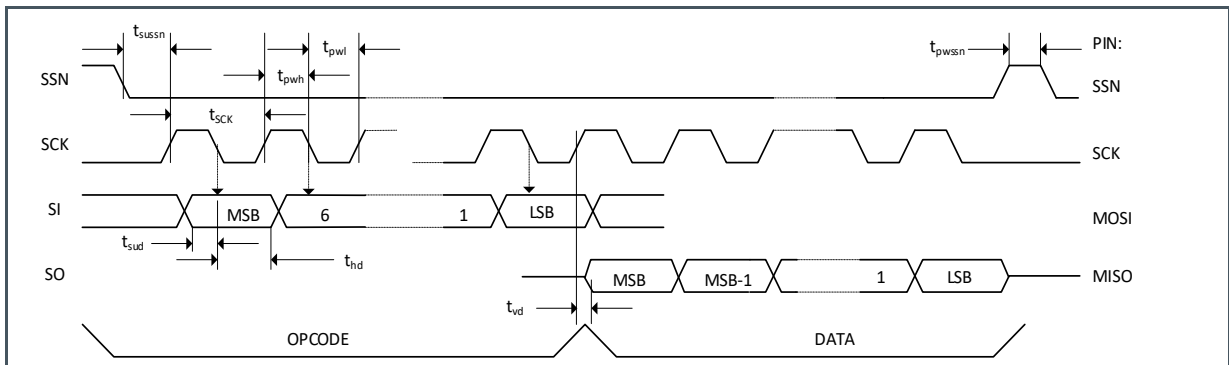


Figure 4:SPI Read



## 6 Detailed Description

### 6.1 Time of flight Measuring Principle

The flow rate of an ultrasonic flow meter is calculated by means of the difference in travel times of ultrasonic bursts. The travel time (time-of-flight) is measured by transmitting digital fire pulses (square waves) on one of the piezoelectric transducer (US-UP) and receiving them (sinus-like waves) on the other piezoelectric transducer (US-DN). The same sequence is then repeated in the opposite direction. The time between transmission and reception is defined as time-of-flight (TOF), the difference between the TOF measured in the 2 directions is the differential time-of-flight (DIFTOF) and it is proportional to the flow speed (water/gas) and can be subsequently calculated by an external microcontroller with the given parameters (length, diameter, speed of sound in water/gas).

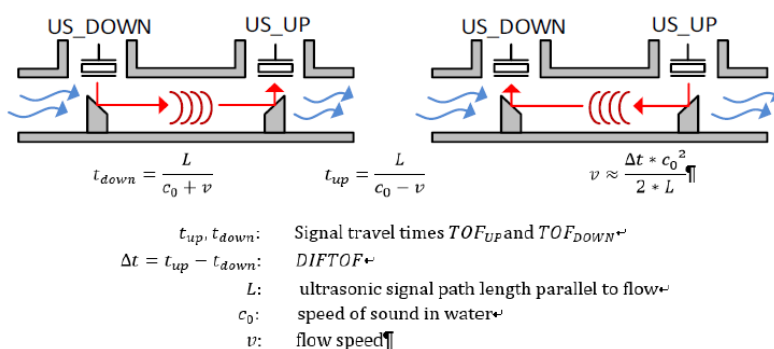


Figure 5: Measuring Principle

The picture above illustrates the measuring principle based on an ultrasonic time of flight (TOF) measurement.

Fire frequency shall be selected in order to match the piezoelectric transducer resonant frequency in order to have an adequate received signal.

### 6.2 Measurement Operations

UFC23 is able to generate the fire burst for the transmission (number of pulses and fire frequency shall be programmed first), and it senses the received burst, translates it into pulses and measures the TOF in up and down direction.

The ultrasonic measurement is supported by following features and sub tasks:

- Control of the LDO and HSO active time
- Fire burst generation based on the HSO
- Single-ended (water) and full-bridge drive options (gas)
- Amplification of the receive signal by an integrated high-gain PGA
- Zero-cross calibrated comparator for first hit level detection and zero-crossing ToF measurement.
- Amplitude measurement and wave monitoring of the ultrasonic receive burst to detect deviations on receiving waveform
- Batch mode allows collection of up to 12 data sets before setting the interrupt
- Temperature measurement with external platinum sensors as required for heat meter or hot water applications

- High speed clock calibration for compensating deviations on nominal frequency of the HSO
- VCC measurement to monitor the battery voltage.
- VDD measurement to monitor the internal LDO output that supplies low voltage circuits.

The ultrasonic measurement and sub-tasks can be triggered by an integrated measure rate generator (self-triggered measure cycle). Alternatively, the measure rate generation can be also served by the external microcontroller via SPI (remote triggered measure cycle).

### 6.2.1 Power-on & Reset

The boot load of the device is always triggered by a reset which can be either a

- Power on reset provided by analog part
- SPI commands: System Reset (comparable with power on reset)

After the reset condition the device automatically enters into a BOOTLOAD state where it executes the first high speed clock measurement and then enters into a STANDBY state.

In this state an interrupt is generated and it is possible to read the status/error flags and to configure the device. Reading the HCC calibration value, stored in RAM, the external microcontroller can calculate which is the external high speed oscillator frequency (4 MHz, 8 MHz, 12 MHz, 16 MHz, 20 MHz) and configure the device according to it.

After the release time for measure mode (  $t_{MM\_RLS}$  ) expires, the device is ready to start the required measurements (self or remote triggered, including calibration measurements).

The LSO takes about 200 ms to settle. 32 ms later communication is possible. The first measurement can start 1 s after the LSO settled.

### 6.2.2 Self Triggered “Measure Cycling”

It is necessary to active the internal timers to start this mode of operation.

Once in STANDBY state (it is not necessary to wait for the  $t_{MM\_RLS}$  ) the device configuration shall be written via SPI and in particular the C\_MCT\_EN (timer mode enable) shall be set and the timers configured to the desired rates (refer to CR\_MRG register). After all the configurations are done the external microcontroller shall send a Measure Mode Control command, setting the measure mode enable bit (EC\_MM\_ENA =1). When both conditions are met ( $t_{MM\_RLS}$  expired and EC\_MM\_ENA =1) the device will move into an INIT state.

In INIT state the following tasks are executed:

- VCC/VDD measurement.
- ZCC: Zero cross calibration if enabled (C\_ZCC\_INIT\_EN)
- HCC: High speed clock calibration

Once completed, the device moves into measurement idle state (MEAS\_IDLE).

In MEAS\_IDLE state the device will receive a trigger every time the timer expires (timer\_cycle\_req) and move into measurement state (MEAS) to execute the measurement tasks. As soon as completed (tsc\_done) it goes back into MEAS\_IDLE waiting for the next trigger.

Only in MEAS\_IDLE state it is possible to read the measurement results stored into the internal RAM (an interrupt is generated at the end of MEAS state).

In MEAS state all the tasks enabled by the timers are executed:

- TOF, WAVE\_AMP: time-of-flight, pulse width and amplitude measurements are controlled by a single rate timer configurable by C\_USM\_RATE. With TOF as the major task, pulse width measurement and amplitude measurement being selected by an individual configuration bit.
- VCC, VDD: VCC and VDD measurement can be controlled by a single rate timer configurable by C\_VM\_RATE.
- ZCC: zero-cross calibration rate is defined by C\_ZCC\_RATE
- HCC: high-speed clock calibration rate is defined by C\_HCC\_RATE
- TEMP: temperature measurement rate is defined by C\_TM\_RATE

To go back into STANDBY state the external microcontroller shall send a Measure Mode Control command, resetting measure mode enable bit (EC\_MM\_ENA =0).

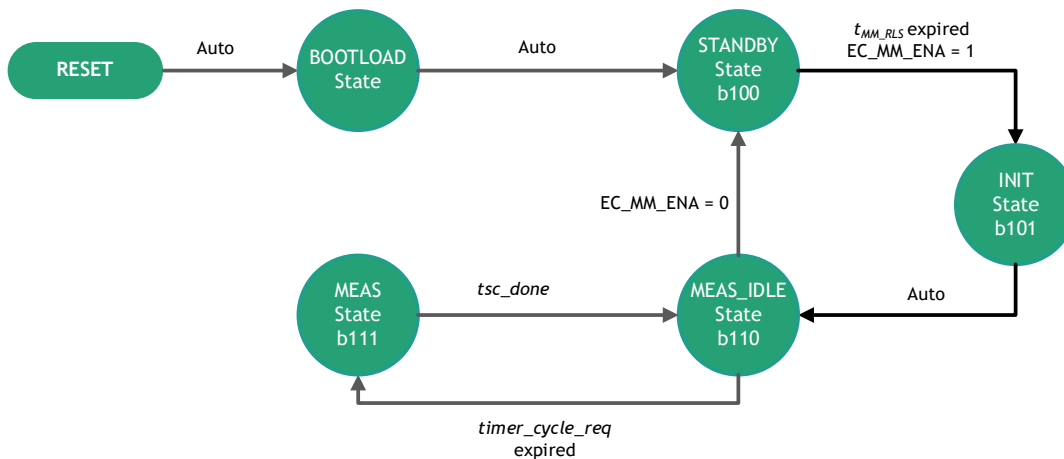


Figure 6: UFC23 state diagram self triggered mode

### 6.2.3 Remote Triggered “Measure Cycling”

The only difference with self-triggered mode is that the internal timers shall not be enabled (C\_MCT\_EN=0).

Once in MEAS\_IDLE state the device will wait for a Cycle Task Request via SPI. As soon as this received, it moves into MEAS state to execute it. Also in this case it is possible to select in the request one or more tasks to be run in sequence (TOF, WAVE\_AMP, VCC, VDD, ZCC, HCC, TEMP, see notes in 6.2.2).

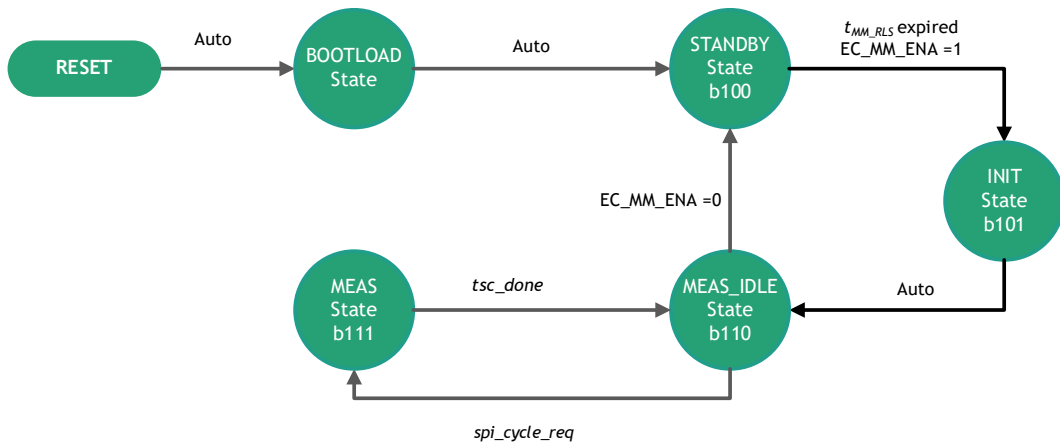


Figure 7: UFC23 state diagram Remote Triggered

### 6.3 Fire Buffers, Receivers & Burst Generation

#### Ultrasonic Interface (UFIC)

Two pairs of drivers are connected to each transducer. The drivers can be programmed for fully differential operation (usually in gas systems) or for single ended operation (usually in water systems).

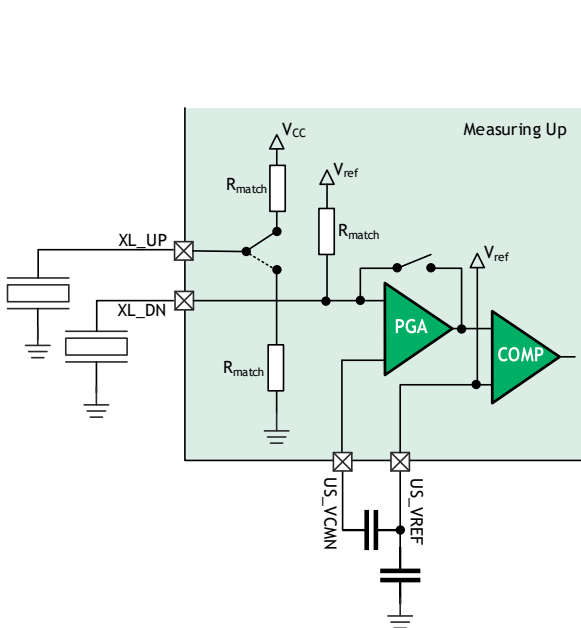


Figure 8: Single-ended transducer drive

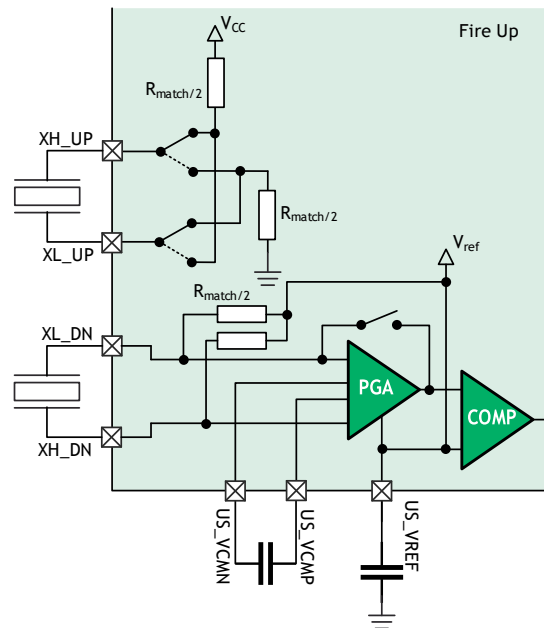


Figure 9: Differential transducer drive

They come with programmable matching resistances for transmission and receiving phases. This means, for fully differential operation there is a range of matching resistances from 64Ω to 1676Ω with a step of 52Ω. For single ended operation the range is from 32Ω to 838Ω with a step of 26Ω.

**Table 9: Single-ended Matching Resistances**

| C_RMSET_TX<br>C_RMSET_RX | R <sub>DRIVE</sub><br>[Ω] | C_RMSET_TX<br>C_RMSET_RX | R <sub>DRIVE</sub><br>[Ω] | C_RMSET_TX<br>C_RMSET_RX | R <sub>DRIVE</sub><br>[Ω] | C_RMSET_TX<br>C_RMSET_RX | R <sub>DRIVE</sub><br>[Ω] |
|--------------------------|---------------------------|--------------------------|---------------------------|--------------------------|---------------------------|--------------------------|---------------------------|
| 0                        | 32                        | 8                        | 240                       | 16                       | 448                       | 24                       | 656                       |
| 1                        | 58                        | 9                        | 266                       | 17                       | 474                       | 25                       | 682                       |
| 2                        | 84                        | 10                       | 292                       | 18                       | 500                       | 26                       | 708                       |
| 3                        | 110                       | 11                       | 318                       | 19                       | 526                       | 27                       | 734                       |
| 4                        | 136                       | 12                       | 344                       | 20                       | 552                       | 28                       | 760                       |
| 5                        | 162                       | 13                       | 370                       | 21                       | 578                       | 29                       | 786                       |
| 6                        | 188                       | 14                       | 396                       | 22                       | 604                       | 30                       | 812                       |
| 7                        | 214                       | 15                       | 422                       | 23                       | 630                       | 31                       | 838                       |

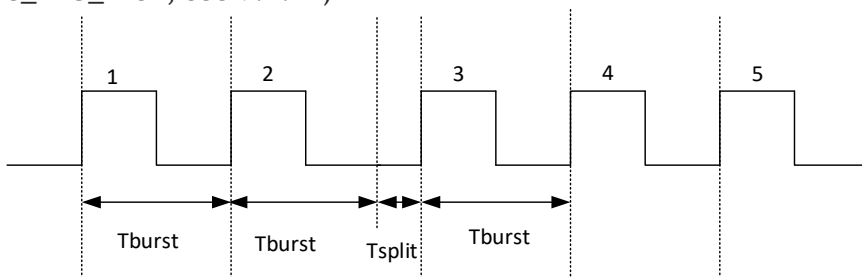
For differential operations the resistance values have to be multiplied by 2.

### 6.3.1 Fire burst generation

The fire burst frequency is derived from the reference by a divider.

$$F\_FIRE = F_{H50} / (2*(C\_FPG\_LR\_CLK\_DIV+1))$$

It is possible to work with split burst, where a programmable low phase is inserted (C\_FSPLITWID, C\_FBG\_FBSP, see 9.2.11)



Phase insertion length is  $T_{split} = N \times T_{burst} / 4$ ,  $N \leq 8$ ,  $T_{burst} = 1 / F\_FIRE$

### 6.3.2 Transducer Open Detection

In UFC23 we implemented a dedicated open transducer detection. The transducer open detection has to be triggered and controlled by the external microcontroller, typically in case there is a timeout situation for a longer period and the user wants to differentiate the hardware error from a simple no-water situation. The chip has to be set to standby, configured with the nominal impedance, and then command RC\_STASK\_REQ has to be sent. In case of an open circuit the bits USM\_HW\_ERR\_UP or USM\_HW\_ERR\_DN in the frontend error flag register will be set.

## 6.4 PGA

The PGA architecture is a two-stage amplifier with the traditional 3 operational amplifier-based architecture. The external capacitance (typ. 10 nF) is needed to achieve unity DC gain on the first stage and minimize the DC offset contribution. The zero-crossing detection shall account for the residual DC offset at the output of the PGA.

The reference voltage of the PGA goes to a pin and is buffered to support the hundreds nF load capacitance. It should be placed as close as possible to the output pad. The reference voltage (input of the buffer) is generated from the voltage reference block. The fixed nominal value is 0.7 V.

### 6.4.1 Single-ended Mode

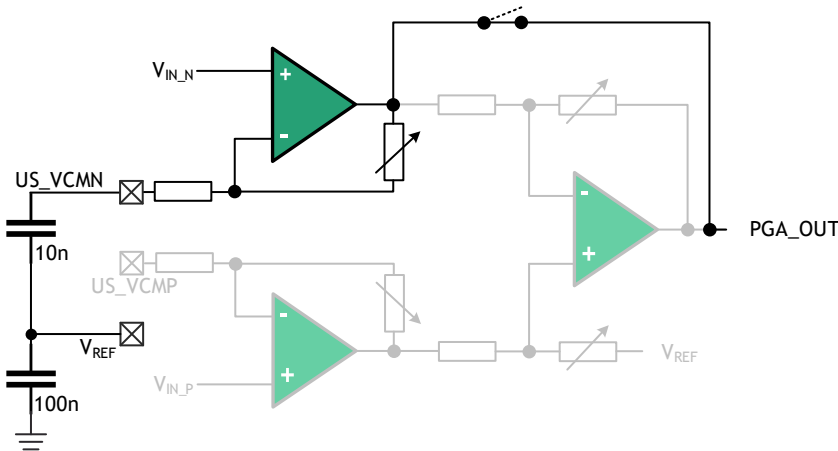


Figure 10: PGA, single-ended

Single-ended configuration is designed to operate in the 0.8 to 4.4 MHz frequency range. The gain for the first stage can be set in 17 steps (C\_PGA\_ST1\_GAIN) for single-ended applications from 2.0 to 10.5 (20.4dB). The second stage is turned off and bypassed.

Table 10: Gain settings single-ended

| Gain1Sel [4:0] | Gain1 | Gain1 [dB] | Gain1Sel [4:0] | Gain1 | Gain1 [dB] |
|----------------|-------|------------|----------------|-------|------------|
| 0              | 2.00  | 6.02       | 8              | 4.51  | 13.08      |
| 1              | 2.21  | 6.90       | 9              | 5.00  | 13.98      |
| 2              | 2.44  | 7.74       | 10             | 5.55  | 14.88      |
| 3              | 2.71  | 8.66       | 11             | 6.13  | 15.75      |
| 4              | 3.00  | 9.54       | 12             | 6.71  | 16.54      |
| 5              | 3.33  | 10.44      | 13             | 7.45  | 17.45      |
| 6              | 3.67  | 11.29      | 14             | 8.14  | 18.22      |
| 7              | 4.08  | 12.21      | 15             | 9.00  | 19.08      |
| 8              | 4.51  | 13.08      | 16             | 9.70  | 19.73      |
| 9              | 5.00  | 13.98      | 17             | 10.52 | 20.44      |

In case no amplification is needed there is the option in single-ended mode to bypass the complete PGA to avoid the consumption of the operational amplifiers. This option is selected by setting  $C\_PGA\_ST1\_CBYP = 1$ .

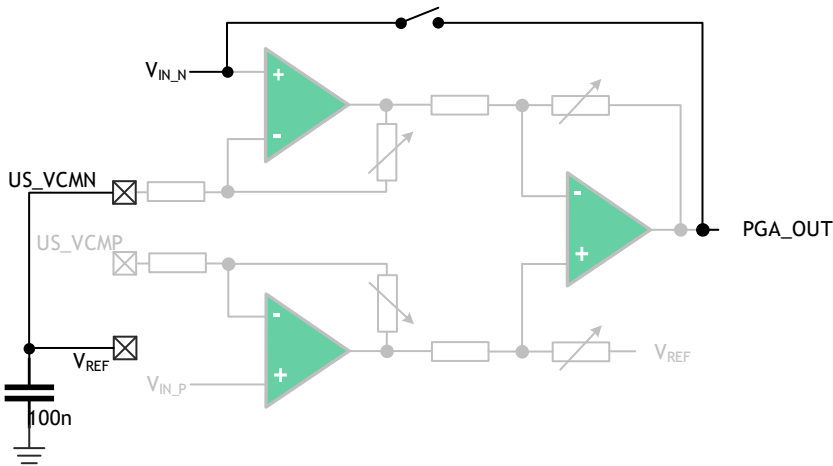


Figure 11: Bypass PGA

### 6.4.2 Differential Mode

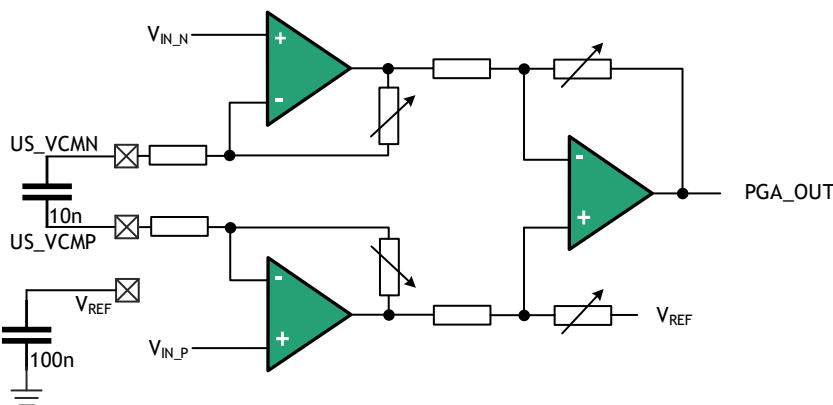


Figure 12: PGA, fully differential

Fully-differential configuration is designed to operate in the 180 to 550 kHz frequency range. The gain of the two stages can be set in the following way:

- 31 steps ( $C\_PGA\_ST1\_GAIN$ ) for the first stage in differential applications from 2.0 to 41 (32dB)
- 4 steps ( $C\_PGA\_ST2\_GAIN$ ) for the second stage with 1, 4, 12 and 24 (27.6dB)

The first stage has to be configured to achieve the largest possible gain; only the residual gain should be provided by the second stage in order to minimize the PGA noise and obtain better stability.

Table 11: Gain settings stage 1, differential

| Gain1Sel [4:0] | Gain1 | Gain1 [dB] | Gain1Sel [4:0] | Gain1 | Gain1 [dB] |
|----------------|-------|------------|----------------|-------|------------|
| 0              | 2.00  | 6.02       | 16             | 9.70  | 19.73      |
| 1              | 2.21  | 6.90       | 17             | 10.52 | 20.44      |
| 2              | 2.44  | 7.74       | 18             | 11.53 | 21.23      |
| 3              | 2.71  | 8.66       | 19             | 12.76 | 22.12      |
| 4              | 3.00  | 9.54       | 20             | 13.50 | 22.61      |
| 5              | 3.33  | 10.44      | 21             | 14.33 | 23.13      |
| 6              | 3.67  | 11.29      | 22             | 15.29 | 23.69      |
| 7              | 4.08  | 12.21      | 23             | 16.38 | 24.29      |
| 8              | 4.51  | 13.08      | 24             | 17.67 | 24.94      |
| 9              | 5.00  | 13.98      | 25             | 19.18 | 25.66      |
| 10             | 5.55  | 14.88      | 26             | 21.00 | 26.44      |
| 11             | 6.13  | 15.75      | 27             | 23.22 | 27.32      |
| 12             | 6.71  | 16.54      | 28             | 26.00 | 28.30      |
| 13             | 7.45  | 17.45      | 29             | 29.57 | 29.42      |
| 14             | 8.14  | 18.22      | 30             | 34.33 | 30.71      |
| 15             | 9.00  | 19.08      | 31             | 41.00 | 32.26      |

Table 12: Gain settings stage 2, differential

| Gain2Sel [1:0] | Gain2 | Gain2 [dB] |
|----------------|-------|------------|
| 0              | 1     | 0          |
| 1              | 4     | 12.04      |
| 2              | 12    | 21.58      |
| 3              | 24    | 27.60      |

### 6.4.3 Unity Gain

In case no amplification is needed there is the option to run the PGA with a gain of one. This will increase the current consumption as the amplifier is added, but in some cases the standard deviation might be improved.

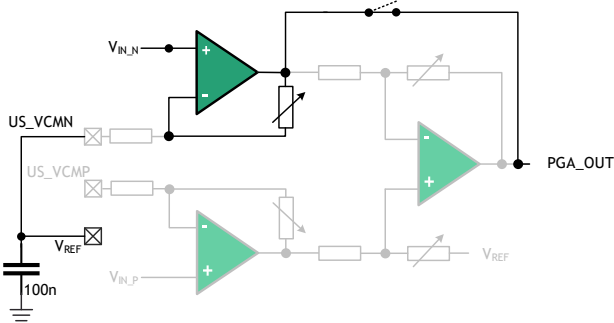


Figure 13: PGA, Unity gain single-ended

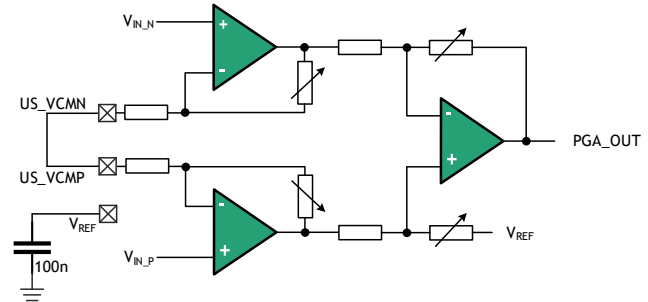


Figure 14: PGA, Unity gain differential

### 6.4.4 PGA Output Monitoring

For test purposes it is possible to have a look to the PGA output on GPIO3 pin. Set the device into standby. Configure GPIO3 as AIO writing 0x00000ADB at the reg CR\_GP\_CTRL (address 0xA2). By default, the config bits (11..9) for GPIO3 are set at b011 and you should write them at b101 when you are enabling the path of the PGAOUT on GPIO3. Then write 0x40002100 at the register address 0xDF (SHR\_debug) to get the PGA out on GPIO3.

The PGAOUT signal visible on GPIO3 is slightly attenuated. This path is useful to understand the shape of the signal received and to understand it is possible to improve something in terms of impedance matching when we are working with small input signal. Any probe at this pin will disturb the measurement itself and therefore this option should be used only for testing the signal shape.

To end the test mode set the device in standby state, write back the original configuration for GPIO3 and send 0x0 to address 0xDF (SHR\_debug).

## 6.5 Time-of-Flight (ToF) Measurement

The steps involved in a single TOF measurement are described here and shown in figures below.

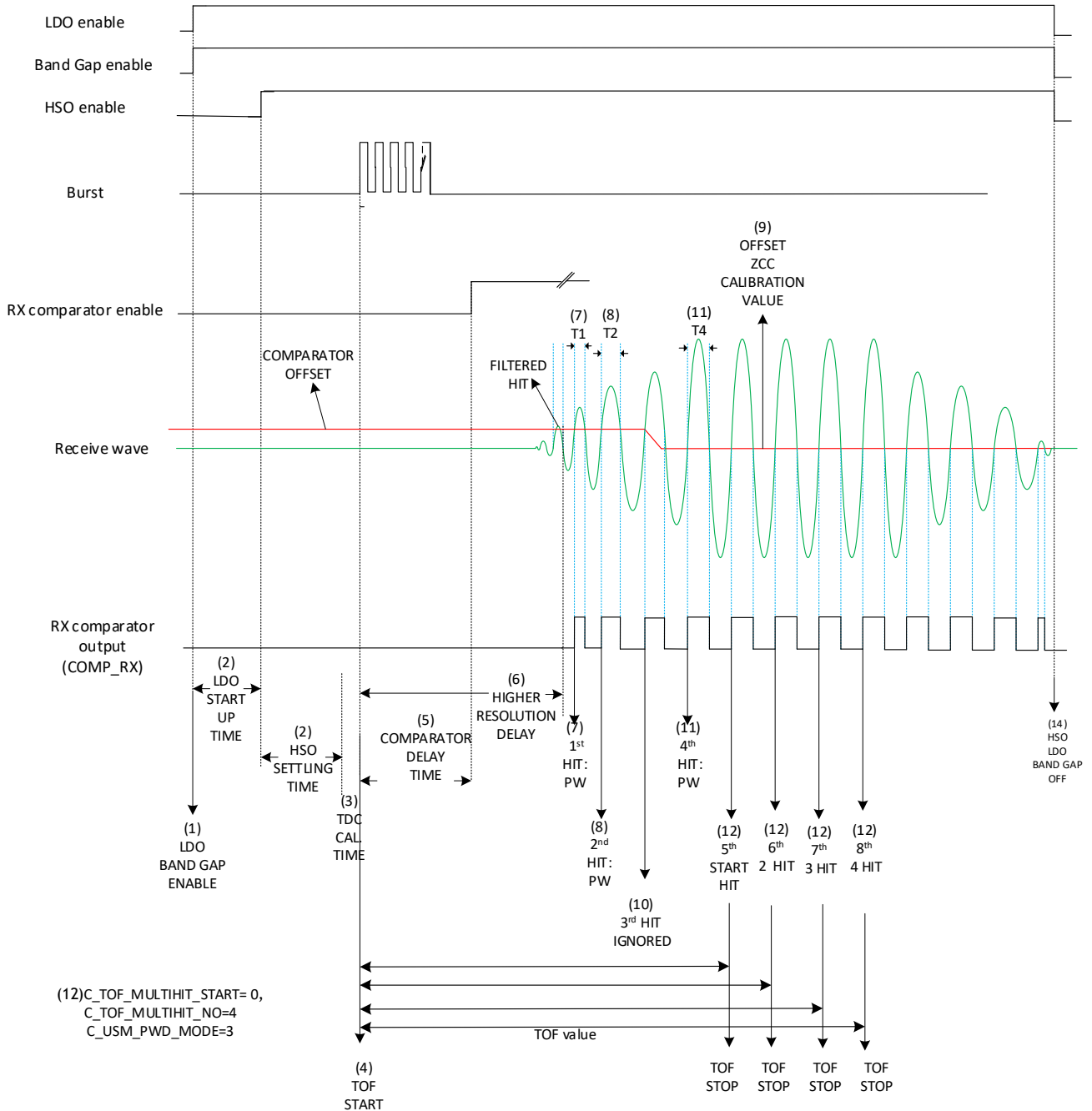


Figure 15: Single ToF measurement sequence

1. The band gap and the LDO are enabled
2. After a programmable LDO startup time (C\_LDO\_STUP\_TSEL[1:0]) also the high speed oscillator (HSO) is turned on. This requires a settling time before stable TDC measurements can be ensured (C\_FEP\_STUP\_TSEL). During this time some analog blocks are turned on (VREF, PGA, DACREF, DAC, COMP) depending on CR\_USM\_RCV\_INIT settings.
3. After the HSO startup the FIRE sequence is started: first of all, a time to digital converter (TDC) calibration is performed (refer to Calibrations chapter) and then a programmable FIRE burst is generated. The number of pulses and the frequency is configurable (CR\_USM\_FBG\_MCTRL). Pulses are generated with a 50% duty cycle. Also the direction UP/DN is programmable (C\_USM\_DIR\_MODE).
4. The first burst pulse rising edge is also the start for the TDC and is used as the time 0 for the TOF measurement.
5. After a programmable delay time (C\_USM\_MASK\_WIN) the device is ready to receive and measure the incoming signals.
6. It is also possible to program a further delay with resolution of  $1/f_{HSO}$ . This can be different for UP or DN measurement direction (C\_USM\_MASK\_HR\_WIN\_UP, C\_USM\_MASK\_HR\_WIN\_DN).
  - a. In this way it is possible to filter unwanted hits at the beginning of the reception phase, after the receive path is enabled and before starting the hit detection by method of first hit regulation.
  - b. With a maximum ratio between HSO frequency and fire frequency, these windows can be also taken to track inside receive burst and to release TOF hits on delay window only as an alternative option to the method of first hit regulation.
7. The first hit is detected when, after all the delays are expired, a wave is received at the comparator input that exceeds the comparator offset voltage with the first hit level setting (C\_USM\_FHL\_UP/ C\_USM\_FHL\_DN). This first hit detected is wave number 1 and its width is measured and stored in RAM.
8. Optionally (C\_USM\_PWD\_MODE[1:0]=11), the same detection is applied also to the second hit (wave number 2)
9. Then the offset of the comparator automatically switches to the ZCC calibration value.
10. The following hit is ignored due to the comparator threshold switching.
11. At this point, if pulse width detection is enabled (C\_USM\_PWD\_MODE[1]), also the pulse width of wave number 4 is measured and stored, otherwise the measurement of the TOF of the received hits is started (START HIT). See 6.5.1 for more details.
12. Received hits are detected and the TOF is measured according to the configured edge (C\_USM\_EDGE\_MODE). It is also possible to select the ignore hit option (C\_TOF\_HIT\_IGN\_MODE) to ignore every second hit. The device is storing the selected hits TOF in the proper RAM location and is also calculating the accumulated TOF results (up to 31 values added up). The number of hits is determined by the parameters:
  - C\_TOF\_HIT\_NO: Number of TOF hits taken TDC measurement
  - C\_TOF\_MULTIHIT\_NO: Number of TOF hits taken for multi-hit summation;
  - C\_TOF\_MULTIHIT\_START: Number of TOF hits (from START hit) before starting multi-hit addition.

13. Once all the expected hits are received (or a timeout is detected), the configured wave amplitudes (up to 3) are then finally calculated (if enabled by C\_USM\_AM\_MODE). The amplitude measurement is performed in 2 parts: Charging capacitor(s) during receive burst, measuring/calculation of capacity load(s) after the receive burst. The capacitance load(s) (up to 3) are determined by a SAR algorithm which can be considered more as a calculation than a measurement. See also section 6.6.
14. At the end the HSO and the analog blocks are turned off.
15. In case C\_USM\_REPEAT is set to measure both directions, the MCT waits for the time interval configured in C\_USM\_PAUSE\_TSEL (from 0.5 to 20 ms) and then starts the full previous sequence in the opposite direction.

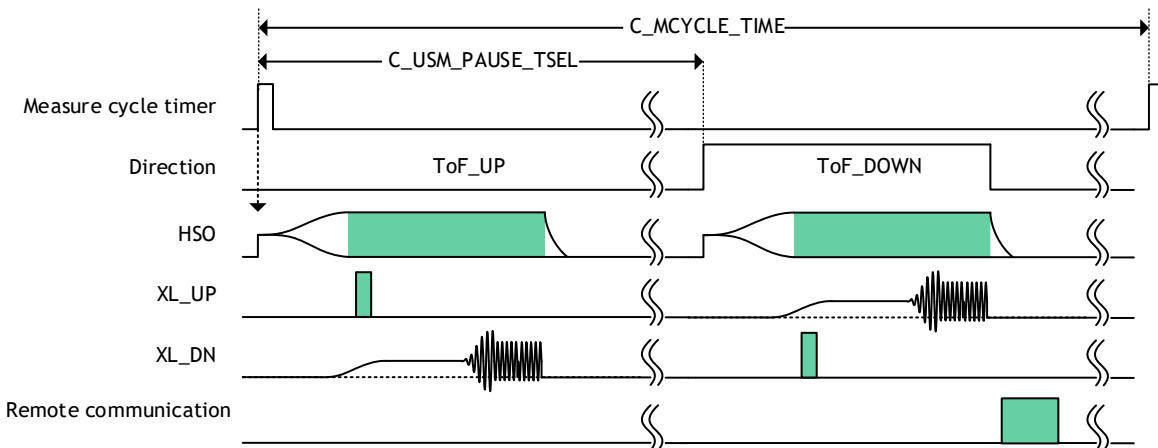


Figure 16: Full Up-Down sequence

### 6.5.1 TOF Calculation

The TDC itself is calibrated against the HSO and the time measurement results, TOF\_DATA is calculated in terms of HSO clock cycles, with 16 bits fractional:

$$LSB_{TOF} = T_{HSO} / 65536$$

### 6.5.2 Pulse Width Detection

There are three options for the pulse width detection. The ratio of pulse width at first hit to pulse width at zero cross level can be used as input for a first hit level regulation.

1) C\_USM\_PWD\_MODE=3

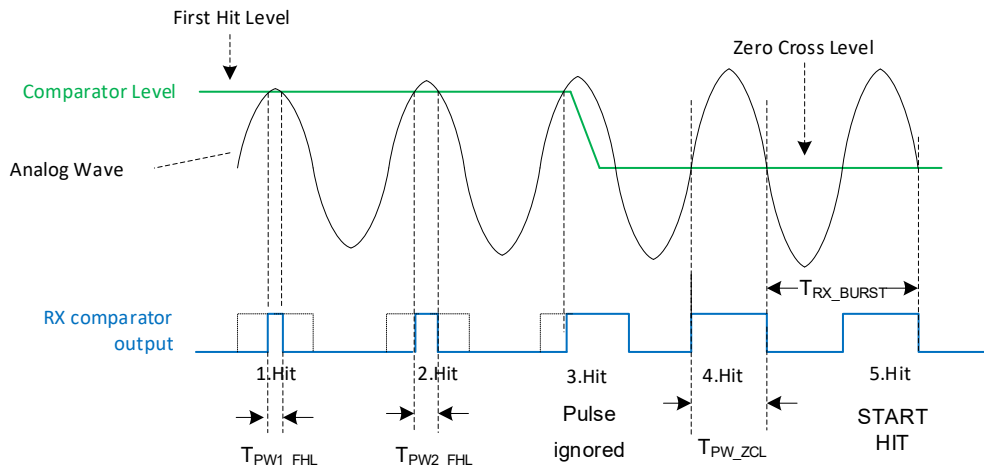


Figure 17: Pulse width detection mode 3

2) C\_USM\_PWD\_MODE=2

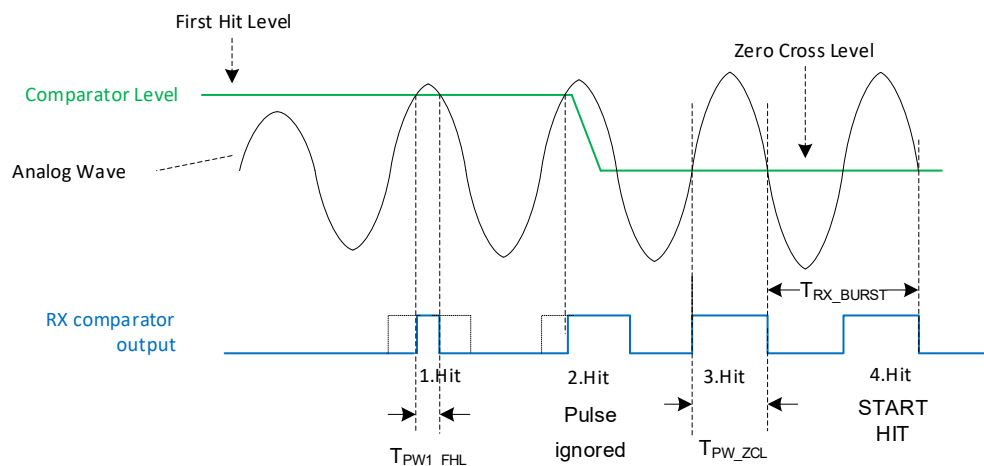


Figure 18: Pulse width detection mode 2

3) C\_USM\_PWD\_MODE=0/1

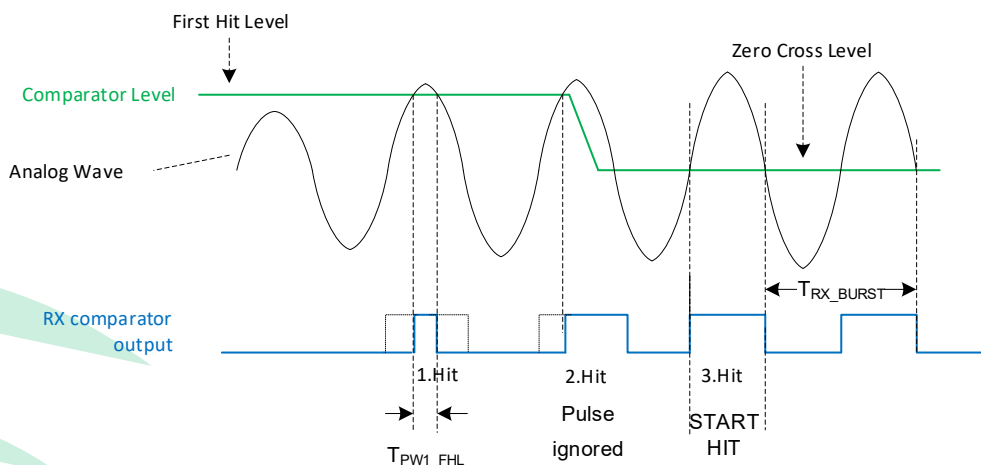


Figure 19: Pulse width detection mode 0 or 1

The PW measurement is done using the high resolution TDC counter only,  $LSB_{PW} = T_{HSO} / 1024$

But the absolute value isn't relevant but the ratios. The following ratio shall be calculated by the external microcontroller:

$$PWR = T_{PW1\_FHL} / T_{PW\_ZCL}$$

Possible PWR range (theoretical):  $0 < PWR < 1$   
 Operational PWR range (for typ. regulation):  $0.5 < PWR < 0.8$

Based on this value it shall be possible to regulate first hit level threshold.

### 6.6 Amplitude Measurement

It is possible to measure the peak amplitude of up to 3 single waves of the receive burst. The three waves (C\_USM\_AM\_PD\_3, C\_USM\_AM\_PD\_2, C\_USM\_AM\_PD\_1) shall be selected in the range 1 to 31 of the received burst .

The peaks of the selected waves are stored during the receiving phase while the conversion is performed right after the TOF measurement. This sequence is performed in same way for both directions (UP/DN), if enabled.

The amplitude is calculated with the same SAR algorithm used for ZCC.

$$LSB_{SAR\_DATA} = 1.4 \text{ V} / 1024 = 1.37 \text{ mV}$$

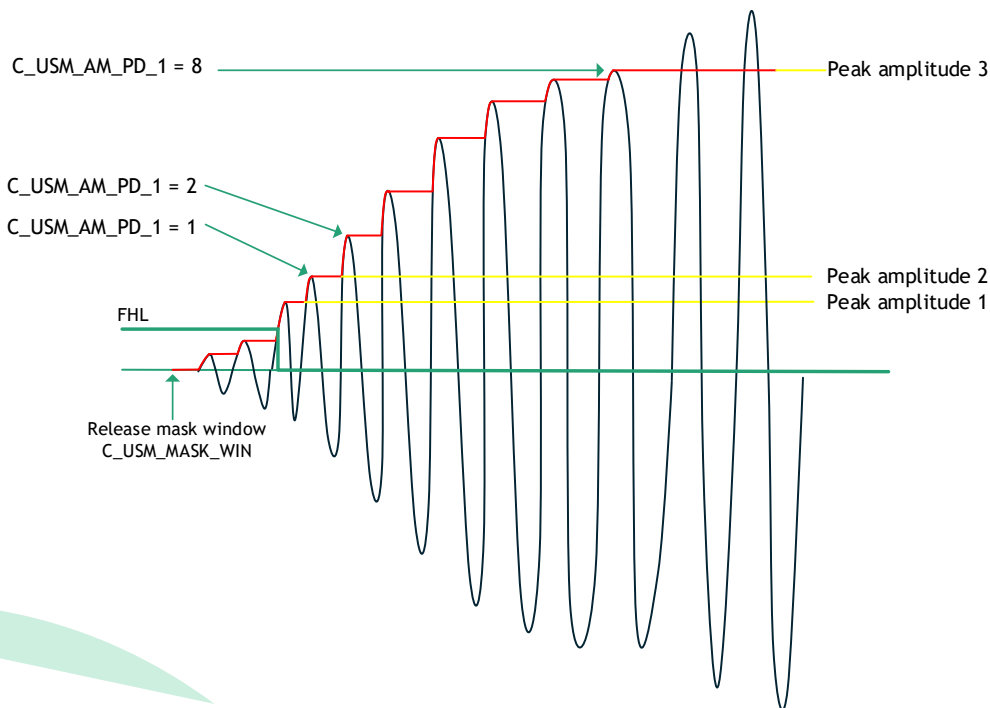


Figure 20: Amplitude measurement

The amplitude measurement is activated when the mask window (low resolution) is released and it takes around 2 us for the activation. The mask window should therefore release early enough.

## 6.7 Sub-Tasks execution

At the end of the second TOF phase all the selected sub-tasks can be performed in the following order:

- ZCC                      Zero cross calibration comparator
- VCC/VDD              Voltage measurement
- HCC                     HSO calibration against LSO
- TEMP                    Temperature measurement

### 6.7.1 Zero-cross Calibration ZCC

Zero crossing calibration is used to compensate the offset of the analog part of the ultrasonic receiving path. It is automatically executed in the INIT state (if enabled).

In self-triggered measure cycling mode it can be performed at the end of the second ultrasonic measurement if enabled via the timers C\_ZCC\_RATE. A calibration every 32 or 64 measurements should be sufficient. In remote-triggered measure cycling mode it can be requested in MEAS\_IDLE state via SPI, using the remote command RC\_CTASK\_REQ + EC\_CTASK\_REQ[1]=1.

Alternatively, it is possible to disable the SAR calibration and write a fixed value into the register C\_ZCD\_LVL.

### 6.7.2 Voltage Measurement

The voltage measurement is for both, VDD and VCC. The measurement rate is set by parameter VCCM\_RATE. The effective bit width is 10 Bits => Bits 15-11 are fixed to 0.

### 6.7.3 High-speed Clock Calibration HCC

For more accurate results, calibration of the HSO upon the accurate 32.768KHz crystal (LSO) can be performed. This is recommended especially because we use ceramic resonators that offer a fast settling but come with observable production variations and temperature drift. Four LSO periods are measured using the same mechanism as TOF measurements.

From the HCC result and T\_LFO value (32.768KHz) it is possible to calculate externally the HFO frequency, considering that:

$$4 * T_{LSO} = 12207031.25 \text{ ps, and } 1 \text{ LSB}_{HSC} = T_{HSO} / 65536.$$

$$HCC = 4 * T_{LSO} * 65536 / T_{HSO} = 64000000 \text{ for } T_{HSO} = 125 \text{ ns}$$

and to calculate the correction factor that shall be used to correct the DIFTOF results:

$$\text{Corr\_factor} = 64000000 / HCC \text{ for } T_{HSO} = 125 \text{ ns}$$

$$\text{DIFTOF\_corr} = (\text{TOF\_UP} - \text{TOF\_DN}) * \text{corr\_factor}$$

It is automatically executed in the BOOTLOAD state and in INIT state.

In self-triggered measure cycling mode it can be performed at the end of the second ultrasonic measurement if enabled via the timers C\_HCC\_RATE.

In remote-triggered measure cycling mode it can be requested in MEAS\_IDLE state via SPI, using the remote command RC\_CTASK\_REQ + EC\_CTASK\_REQ[3]=1.

## 6.8 Temperature Measurement

UFC23 is equipped with a highly accurate 2-wire interface for resistive temperature sensors. Resistive measurements are based on discharge time measurements, using a fixed load capacitor discharged sequentially through the sensor resistors and a reference resistor. The sensors' resistance is defined by calculating the ratio of sensors' discharge time and reference resistor's discharge time.

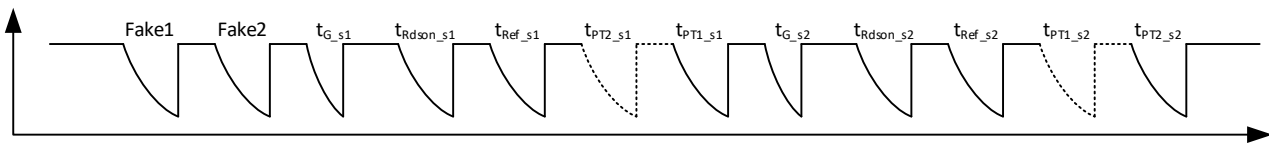


Figure 21: Temperature measurement

For precision temperature measurement with mK precision, as needed in heat meters, platinum resistors (PT500 or PT1000) are recommended. The external load capacitor should be of COG material. One discharge cycle takes a time of about

$$\tau = 0.7 \times R \times C_{Load}$$

This makes e.g. 70  $\mu$ s for a 1 k $\Omega$  resistor R and a 100 nF capacitor  $C_{load}$ .

Heat meters will need two sensors, for hot water (incoming) and cold water (outcoming). Water meters will need a temperature sensor only in case of hot water meters with temperatures above 60°C. In cold water meters the temperature can be calculated from the sum of time-of-flight.

The mode selection will define the sequence of the activation of the internal switches. This includes also compensation measurements that correct for  $R_{ds(on)}$  (switch resistance) and gain (comparator delay).

A measurement sequence for 2 sensor looks like the following:

- 1) 1<sup>st</sup> fake measurement. The capacitor is discharged without any time measurement. This is to stabilize the load capacitor.
- 2) 2<sup>nd</sup> fake measurement
- 3)  $t_{gain}$  for the gain compensation, with the switches at TM\_REF and TM\_PT1 being closed
- 4)  $t_{Rdson}$  for the  $R_{ds(on)}$  compensation, measuring at pin TM\_REF
- 5)  $t_{REF}$  for the reference at pin TM\_REF by closing the full switch.
- 6)  $t_{PT2}$  is measured discharging the capacitor with the resistor at pin TM\_PT2. This step is skipped in case of a single sensor application.
- 7)  $t_{PT1}$  is measured discharging the capacitor with the resistor at pin TM\_PT1
- 8) Optional repetition of sequence 3. to 7. in reversed order.

Results of these five measurements are stored in the data buffer, from address 144 to 153.

The following configuration options are implemented:

- 1 or 2 measure ports (C\_TM\_PORT\_NO)
- Cycle Time (C\_TM\_CYCLE\_SEL)
- Inactive Port Mode, GND or High-Z (C\_TM\_PORT\_MODE)
- 1 or two sequences, 2<sup>nd</sup> one in reversed port order (C\_TM\_SQC\_NO)

In self-triggered measure cycling mode, the temperature measurement can be performed directly at the end of the second ultrasonic measurement if enabled via the timers C\_TM\_RATE.

In remote-triggered measure cycling it can be requested in MEAS\_IDLE state via SPI using the remote command RC\_CTASK\_REQ + EC\_CTASK\_REQ[5]=1.

### 6.8.1 Temperature calculation

The RAM holds the following data:

$t_{G\_s1}$ ,  $t_{Rdson\_s1}$ ,  $t_{Ref\_s1}$ ,  $t_{PT1\_s1}$ ,  $t_{PT2\_s1}$  and eventually for the 2<sup>nd</sup> sequence  $t_{G\_s2}$ ,  $t_{Rdson\_s2}$ ,  $t_{Ref\_s2}$ ,  $t_{PT1\_s2}$ ,  $t_{PT2\_s2}$

The raw results given here are TDC values. They can be converted to actual times by multiplying with  $T_{HSO}/2^{16}$ . But since in the final calculation only ratios of values will be used, this conversion into time is not needed.

$t_{PT1\_sx}$ ,  $t_{PT2\_sx}$  and  $t_{REF\_sx}$  correspond to the total resistance values of the measured network, including internal switch resistances. To remove the influence of switch resistances and comparator delay, measurements  $t_{Rdson\_sx}$  "and"  $t_{G\_sx}$  should be used according to the following equations<sup>8</sup>:

$t_{ds(on)}$  correction (the correction of switch resistances)  $t_{RO} = t_{Rdsom\_sx} - t_{Ref}$

Schmitt trigger delay compensation<sup>9</sup> 
$$\Delta t = 2 \times t_{G\_sx} - 2 \times \frac{t_{PT1\_sx} \times t_{Ref\_sx}}{t_{PT1\_sx} + t_{Ref\_sx}}$$

Note that the Schmitt trigger delay compensation requires a measurement of the TM\_PT1 sensor. In case one sensor may be optional, always use the PT1 sensor for the optional one.

Reference:  $t_R = t_{REF\_sx} - t_{RO} - \Delta t$

Sensors PT1:  $t_1 = t_{PT1\_sx} - t_{RO} - \Delta t$

PT2:  $t_2 = t_{PT2\_sx} - t_{RO} - \Delta t$

The sensor to reference ratios are used in the following for the temperature calculation:

<sup>8</sup> The calculation assumes that all double switches are identical, and that the measurements are linear and repeatable. Under these conditions, the sensor network resistances are measured to the accuracy of the reference resistor, with an uncertainty through added noise of  $\pm 0.001\%$  of full scale. Additional line resistances in the sensor networks can't be calibrated out by 2-Wire measurements. If the line resistances are known from different measurements, they may simply be subtracted from the result in a separate calibration.

<sup>9</sup> The calibration measurement for comparator delay uses the cold sensor. If the cold sensor path is unusable, for example due to some damage, also the hot sensor path can't be fully calibrated. So, if only one sensor is used, always use the cold sensor pins, and if one sensor result is needed with high accuracy, even in case the other sensor may be damaged, connect the more important sensor to the cold sensor ports

Sensor resistance vs. reference:

$$R_1 \text{ (e.g. cold): } \quad R_1 = \frac{t_1}{t_R} \times R_{Ref} \quad R_2 \text{ (e.g. hot): } \quad R_2 = \frac{t_2}{t_R} \times R_{Ref}$$

The calculation of temperatures from resistance values is done as usual through the sensor's characteristic T(R) curve. A simplified polynomial resembles the inverted R(T)-polynomial for PT (according to IEC 60751:2008) within 0°C and 100°C.

$$\text{Temperature } T[^\circ\text{C}] = 10.115 \times \left(\frac{t_{1,2}}{t_R}\right)^2 + 235.57 \times \left(\frac{t_{1,2}}{t_R}\right) - 245.683 \quad \text{Format: fd16}$$

## 6.9 TOF Error Handling

### 6.9.1 Timeout

TDC fine counter timeout and USM timeout are detected.

TDC fine counter timeout appears when no TDC stop arrives after the TDC's maximum value. This should not appear under normal conditions and indicates a major system issue.

USM timeout is detected when the expected number of pulses is not received within C\_USM\_TMO\_SEL from the first FIRE pulse. This typically happens when the receive signal is too small to pass the first hit level detection or when there is no receive signal at all. Common root causes for this error are no water in the tube or a broken transducer connection.

### 6.9.2 VCC,VDD Under-voltage

The VCC and VDD measurement is performed by an SAR algorithm. Measured values are stored in the RAM and are available to the external  $\mu\text{C}$  that can discard the related measurements in case they are too low.

It is automatically executed in the INIT state.

In self-triggered measure cycling mode it can be performed at the end of the second ultrasonic measurement if enabled via the timers C\_VM\_RATE.

In remote-triggered measure cycling it can be requested in MEAS\_IDLE state via SPI, using the remote command RC\_CTASK\_REQ + EC\_CTASK\_REQ[2]=1.

### 6.9.3 Temperature Ports Open & Short

Temperature pins connection open and short conditions are detected during temperature measurement.

### 6.9.4 Transducer Ports Open

The spool piece error handling can be requested only during STANDBY state via SPI using the service task request command RC\_STASK\_REQ[3:0]. So, coming from MEAS state, the measure mode enable shall be reset (EC\_MM\_ENA =0). Before sending this command the user shall program the matching resistance as described on chapter 6.3.2 and CR\_USM\_FBG\_MCTRL shall maintain the settings used for firing.

## 6.10 Batch mode

If enabled ( $C\_USM\_MHIT\_BATCH \geq 1$ ) it is possible to collect TOF multi hits over several measure cycles before providing an interrupt to remote controller. The PW, amplitude and errors information are stored too (refer to Random Access Area mapping).

## 6.11 Interrupts and flags

Flag register are readable via SPI (Refer to SPI command “Flag Registers Read”) independent from state of internal system bus, with the exception of Frontend status and error flags, that will return 0 if read while the Frontend block is running and it is updating the flags (BOOTLOAD, INIT and MEAS states). Refer to Communication flag register.

It is strongly recommended to have an interrupt-based communication via INTN, as any SPI communication during a measurement can have a negative impact on the measurement quality.

Refer to Communication Sequences chapter.

### 6.11.1 Communication Flag Register

*Table 13: Communication flags*

| Bit | Description   | Behaviour <sup>10</sup> |
|-----|---|-------------------------|
| 0   | System Bus Master State: 0: SPI can access entire memory without bus collision, 1: FEP front-end processing ongoing | CS                      |
| 1   | System Bus Collision: 1: Collision was Detected   | LS                      |
| 2   | Task execution: 0: IDLE, 1: BUSY  | CS                      |
| 3   | Measure Cycle Timer Tail Time   | CS                      |
| 6   | CR update error   | LS                      |
| 7   | Error Flag: OR of error flag register   | CS                      |

An uncritical communication is characterized by reading back 0x00 for this .

Bit 1 is set in case of collision: Collision is detected in case an SPI access to RAM or to Frontend Status/Error Flag registers is performed while bit 0 is 1 (Frontend block is using the bus). In case of collision the SPI data output (SPI\_MISO) is forced to 0.

Bit 3, tail time flag, can be used to estimate whether the remaining time before the next measure cycle is long enough for a planned communication. This needs to be estimated based on the number of data that will be read.

<sup>10</sup> CS: flag shows current status, LS: latched flag, cleared by a dedicated clear command

Bit 6 is set in case a configuration register is written when not allowed (explicitly when not in MCYCLE\_IDLE state) to indicate that the new value, also if written into the register, was not used and shall be written again. This happens for example in case the MCYCLE\_IDLE is going to 0 immediately after the write and the new value cannot be propagated to the LF domain. Moreover it is set in case an SPI activity is detected (SPI CSN low) before the release of the FEP clock/reset, causing the release to be delayed till SPI idle.

### 6.11.2 Interrupt Flag Register

Following interrupt requests are enabled by default (CR\_FRU\_I EH), but can be selectively disabled via configuration setup. The register can be cleared for all bits in common by a dedicated SPI command (“Flag Register Clear -> EC\_IF\_CLR=1”). There is no automatic clear when register is read.

Except for bit 7, depending on their enabling status they are combined to a common interrupt forwarded to INTN: so INTN is driven low as soon as one of these bits is set and enabled.

Bit 7 is for info only, it doesn’t cause any interrupt.

*Table 14: Interrupt flags*

| Bit | Description   | Behaviour |
|-----|---|-----------|
| 0   | Bootload Sequence Done  | LS        |
| 1   | Measure Init Sequence Done  | LS        |
| 2   | Measure Cycle Sequence Done   | LS        |
| 3   | Measure Cycle Batch Done  | LS        |
| 4   | Service Task Request Done<br>Ultrasonic Error Handling  | LS        |
| 5   | USM_PAUSE_ERR: ultrasonic measure sequence not finished within configured pause time (C_USM_PAUSE_TSEL) | LS        |
| 6   | Task Timeout (new task requested before the previous was completed)                                     | LS        |
| 7   | Error Detected (refer to Error Flag register for details)   | LS        |

### 6.11.3 Frontend Error Flag Register

Table 15: Frontend error flags

| Bit | Description  | Behaviour |
|-----|--|-----------|
| 0   | TDC_TO_HCC: TDC counter timeout detected during HCC measurement  | LS        |
| 1   | TDC_TO_TM: TDC counter timeout detected during temperature measurement   | LS        |
| 2   | TM_OPEN: 0 = short on any active TM port, 1 = at least one open error on an active TM port   | LS        |
| 3   | TM_SHORT: 0 = no TM error. 1 = TM error, either short or open  | LS        |
| 4   | USM_HW_ERR_UP: USM HW error detected in up direction   | LS        |
| 5   | USM_HW_ERR_DN: USM HW error detected in down direction   | LS        |
| 6   | TDC_TO_PW_UP: TDC counter timeout detected during Pulse Width meas. in up direction  | LS        |
| 7   | TDC_TO_PW_DN: TDC counter timeout detected during Pulse Width meas. in dn direction  | LS        |
| 8   | TDC_TO_TOF_UP: TDC counter timeout detected during TOF measurement in up direction   | LS        |
| 9   | TDC_TO_TOF_DN: TDC counter timeout detected during TOF measurement in dn direction   | LS        |
| 10  | USM_TO_TOF_UP: number of expected TOF hits (single or multi) not received before the programmed timeout (defined by C_USM_TMO_SEL) in up direction   | LS        |
| 11  | USM_TO_TOF_DN: number of expected TOF hits (single or multi) not received before the programmed timeout (defined by C_USM_TMO_SEL) in down direction | LS        |

Error flag are from bit 0 to bit 11. Each error flag can be enabled separately (CR\_FRU\_EFH). All enabled flags can be combined and provided as a common “Error Flag” which is provided to the other flag register for read.

Flags can be read only while the FEP is not accessing to the bus (System Bus Master State = 0 in the communication flag register).

Bits are set as soon as the condition is verified, they are reset by a dedicated SPI command (“Flag Register Clear -> EC\_EF\_CLR=1”).

The frontend error flag register shall be used only when UFC23 is operating in single cycle mode. When operating in batch cycle mode the frontend error flags have to be read from relative address +11 of each USM bundle which is also valid when operating in single cycle mode.

#### 6.11.4 Frontend Status Flag Register

Additional flags are provided as info via SPI command “Flag Registers Read”. These flags can be read only while the FEP is not accessing to the bus (System Bus Master State = 0 in the communication flag register). Bits are set as soon as the condition is verified, they are reset by a dedicated SPI command (“Flag Register Clear -> EC\_FES\_CLR=1”).

*Table 16: Frontend status flags*

| Bit | Description  | Behaviour |
|-----|--|-----------|
| 0   | HCC result updated                                       | LS        |
| 1   | ZCC result updated                                       | LS        |
| 2   | VCC/VDD result updated                                   | LS        |
| 3   | Temperature results updated                              | LS        |
| 4   | USM-UP results updated                                   | LS        |
| 5   | USM-DN results updated                                   | LS        |
| 6   | Ultrasonic Error Handling updated                        | LS        |
| 7   | Frontend Error Flag: OR of error flag register bits 11-0 | LS        |

The Frontend Status Flag Register shall be used only when UFC23 is operating in single cycle mode. When operating in batch cycle mode the frontend status flags have to be read from relative address +11 of each USM bundle which is also valid when operating in single cycle mode.

#### 6.11.5 System Status Flag Register

*Table 17: System status flags*

| Bit | Description  | Behaviour |
|-----|--|-----------|
| 0   | LSO Settled (LS_STUP_TMO): LSO startup timer timeout               | CS        |
| 1   | Main State [2]: Main State is Standby or INIT or MEAS_IDLE or MEAS | CS        |
| 2   | BL_REQ: bootload main state  | CS        |
| 3   | MIS_REQ: Init main state   | CS        |
| 4   | MCYCLE_REQ: MEAS_IDLE or MEAS state                                | CS        |
| 5   | MCT Halt State: timer halt requested via SPI                       | CS        |

|   |                                       |    |
|---|---------------------------------------|----|
| 6 | HSO TMO: HSO not connected            | CS |
| 7 | Error Flag: OR of error flag register | CS |

These flags indicates the current status of the FSM and cannot be cleared via SPI reset commands

## 7 Host communication

The UFC23 operates as a sub (slave) device integrable in a multi-target SPI interface.

Communication with UFC23 is always triggered from the SPI main controller by sending a remote command as the first byte of a remote request.

The SPI sub controller of UFC23 has to handle following different transfers separated in different categories (write/read direction referred to SPI main controller):

*Table 18: Communication categories*

| Transfer Category   | Write: M->S                                    | Read: S->M     | Comment  |
|---|--|----------------|--|
| Task Execution:   | 2 CMD-Bytes                                    |                | <ul style="list-style-type: none"> <li>- Reset Management</li> <li>- Flag Register Clearing</li> <li>- Measure Mode Control</li> <li>- Main Task Request</li> <li>- Cycle Task Request</li> </ul>  |
| Read Status Flag Register:                                  | 2 CMD-Bytes                                    | PL-Byte * n    | <ul style="list-style-type: none"> <li>- Communication Flag Register (1)</li> <li>- Interrupt Flag Register (1)</li> <li>- Frontend Error Flag Register (2)</li> <li>- Frontend Status Flag Register (1)</li> <li>- System Status Flag Register (1)</li> </ul> |
| System Bus Access:<br>Write Data<br>into Random Access Area | 1 CMD/ADR-Byte<br>1 ADR-Byte<br>4 PL-Bytes * n |                | Block Transfer (4-byte-wise)   |
| System Bus Access:<br>Read Data<br>from Random Access Area  | 1 CMD/ADR-Byte<br>1 ADR-Byte                   | 4 PL-Bytes * n | Block Transfer (4-byte-wise)   |

CMD: Command  
M: Main

ADR: Address  
S: Sub

PL: Payload

Address is incremented after each 4-byte-data transfer. Byte contents are always transferred with most significant bit first. Payload data or status is always transferred with most significant byte first.

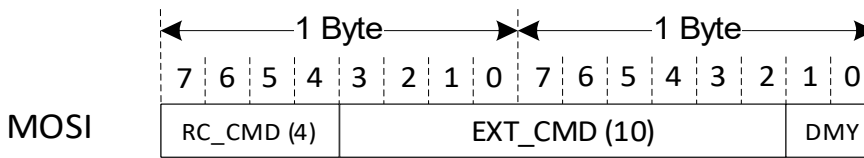
Table 19: Communication acronyms

| Acronym | Remote Command                              | Length   |
|---------|---|----------|
| RC_     | Remote Command                              | 4 Bit    |
| EC_     | Extended Command                            | 10 Bit   |
| DMY     | Dummy Bits (don't care status)              | 2 Bit    |
| PL_     | Payload (only for Get Status Flag Register) | 1-6 byte |

## 7.1 Task Execution

For “Task Execution” a remote command RC\_xxxx\_xxx is always followed by an extended command EC\_xxxx\_xxx and the 2 dummy bits.

Figure 22: Reset Management Request: Remote Command



### 7.1.1 Reset Management

Decoded commands are forwarded to module “Reset Management”.

Table 20: Reset Management Request: Remote Command

| Remote Command | Code  | Description              |
|----------------|-------|--------------------------|
| RC_RM_REQ[3:0] | b0101 | Reset Management Request |

Table 21: Reset Management Request: Extended Command

| Extended Command | Description  |
|------------------|--|
| EC_RM_REQ[9:0]   | Reset Management Request<br>[9:8] b00: <i>not used</i><br>[7:0] 0xAA EC_SYS_RST: Resets all digital blocks<br>0xAC EC_CR_INIT: Resets Configuration register |

- Each reset command can be performed exclusive only

- After command is provided by external MCU, reset task is performed directly without any further command required for releasing reset. In case the same EC\_RM\_REQ shall be sent consecutively, it shall be separated by a reset command with EC\_RM\_REQ=0.  
Ex. 0x52A8 , 0x5000, 0x52A8
- A latency of 100us shall be respected between 2 consecutive Reset commands.

### 7.1.2 Flag Register Clear

Decoded commands are forwarded to module “Flag Register Unit”.

Table 22: Flag Register Clear: Remote Command

| Remote Command  | Code  | Description         |
|-----------------|-------|---------------------|
| RC_FRU_CLR[3:0] | b1011 | Flag Register Clear |

Table 23: Flag Register Clear: Extended Command

| Extended Command | Description   |
|------------------|---|
| EC_FRU_CLR[9:0]  | Flag Register Clear<br>[9:5] b00000: <i>not used</i><br>[4] not used<br>[3] EC_FES_CLR: Clears Frontend Status Flag Register<br>[2] EC_EF_CLR: Clears Frontend Error Flag Register<br>[1] EC_IF_CLR: Clears Interrupt Flag Register<br>[0] EC_CMF_CLR: Clears Communication Flag Register |

- *Clear command bits can be combined arbitrary.*
- *After command is provided by external MCU, clear task is performed directly without any further command required for releasing clear.*
- *Provide the command followed by the Reset command with extended command = 0x00. A latency of 100us shall be respected between 2 consecutive flag register clear commands.*

### 7.1.3 Measure Mode Control

Decoded commands are forwarded to module “Measure Mode Control & Task Requester”.

Table 24: Measure Mode Control: Remote Command

| Remote Command  | Code  | Description          |
|-----------------|-------|----------------------|
| RC_MM_CTRL[3:0] | b0011 | Measure Mode Control |

Table 25: Measure Mode Control: Extended Command

| Extended Command | Description  |
|------------------|--|
| EC_MM_CTRL[9:0]  | Measure Mode Control<br>[9:4] b00000: <i>not used</i><br>[3] '0': EC_MRG_CLR: Measure Rate Generator Released<br>'1': EC_MRG_CLR: Measure Rate Generator Clear<br>[2] '0': EC_MCT_CLR: Measure Cycle Timer Released<br>'1': EC_MCT_CLR: Measure Cycle Timer Clear<br>[1] '0': EC_MCT_HALT: Measure Cycle Timer Released<br>'1': EC_MCT_HALT: Measure Cycle Timer Halt<br>[0] '0': EC_MM_ENA: Measure Mode Disabled<br>'1': EC_MM_ENA: Measure Mode Enabled |

- Measure mode control command bits can be combined arbitrary.
- Command bits have a “toggling state” character: After a command bit is provided by external MCU, opposite meaning of bit has to be provided again to change the state..
- A latency of 100us shall be respected between 2 consecutive Measure mode commands .

### 7.1.4 Service Task Request

Decoded commands are forwarded to module “Task Requester”.

Table 26: Service Task Request: Remote Command

| Remote Command    | Code  | Description          |
|-------------------|-------|----------------------|
| RC_STASK_REQ[3:0] | b0110 | Service Task Request |

Table 27: Service Task Request: Extended Command

| Extended Command  | Description   |
|-------------------|---|
| EC_STASK_REQ[9:0] | Service Task Request<br>[9:8] b00: <i>not used</i><br>[7:0] 0xE2 EC_EHSP_REQ: Error Handling: Spool Piece |

- After command is provided by external MCU, task request is performed directly without any further command required for finishing task request.
- End of task request typically flagged by interrupt.

### 7.1.5 Cycle Task Request

Decoded commands are forwarded to module “Task Requester”.

*Table 28: Cycle Task Request: Remote Command*

| Remote Command    | Code  | Description        |
|-------------------|-------|--------------------|
| RC_CTASK_REQ[3:0] | b0111 | Cycle Task Request |

*Table 29: Cycle Task Request: Extended Command*

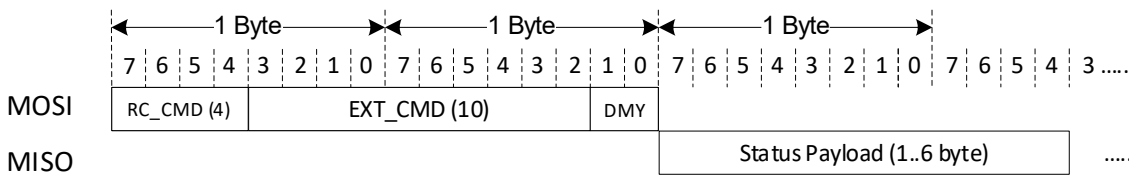
| Extended Command | Description  |
|------------------|--|
| EC_CTASK_REQ     | Cycle Task Request<br>[9:6] b000: <i>not used</i><br>[5] EC_TM_REQ: Temperature Measurement Request<br>[4] <i>not used</i><br>[3] EC_HCC_REQ: High Speed Clock Calibration Request<br>[2] EC_VCCM_REQ: VCC/VDD Measurement Request<br>[1] EC_ZCC_REQ: Zero Cross Calibration Request<br>[0] EC_USM_REQ: Ultrasonic Measurement Request |

- *These task requests by remote controller can be optionally provided as triggered by “Measure Rate Generator”.*
- *Request command bits can be combined arbitrary.*
- *Command bits have a “trigger” character: After command is provided by external MCU, request tasks are performed directly without any further command required for finishing request.*
- *End of task request typically flagged by interrupt.*

## 7.2 Flag Register Read

For “Flag Register Read” a remote command RC\_xxxx\_xxx is always followed by an extended command EC\_xxxx\_xxx and the 2 dummy bits . As an answer flag register contents are sent back as status payload.

Figure 23: Flag Register Read



Payload order of flag register is oriented to order in extended command:

- Communication Status Register: 1 byte
- Interrupt Flag Register: 1 byte
- Frontend Error Flag Register: 2 bytes
- Frontend Status Flag Register: 1 byte
- System Status Flag Register: 1 byte

Decoded commands are forwarded to module “Flag Register Unit”.

Table 30: Flag Register Read: Remote Command

| Remote Command | Code  | Description        |
|----------------|-------|--------------------|
| RC_FRU_RD[3:0] | b1001 | Flag Register Read |

Table 31: Flag Register Read: Extended Command

| Extended Command | Description   |
|------------------|---|
| EC_FRU_RD[9:0]   | Flag Register Clear<br>[9:5] b00000: <i>not used</i><br>[4] RC_SSF_RD: Read System Status Flag Register<br>[3] RC_FSF_RD: Read Frontend Status Flag Register<br>[2] RC_FEF_RD: Read Frontend Error Flag Register<br>[1] RC_IF_RD: Read Interrupt Flag Register<br>[0] RC_CMF_RD: Read Communication Flag Register |

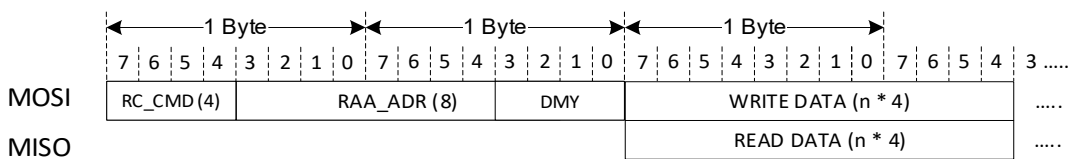
- Read command bits can be combined arbitrary.
- Starting from bit [0], status register contents are read in ascendant order as selected.

### 7.3 Random Area Access

Table 32::Acronyms

| Acronym    | Remote Command                | Length                   |
|------------|-------------------------------|--------------------------|
| RC_RAA_    | Remote Command RAA            | 4 Bit                    |
| RAA_ADR    | Random Access Area Address    | 8 Bit                    |
| RAA_WDx_Bx | Random Access Area Write Data | ≥ 4 Bytes (4 bytes wise) |
| RAA_RDx_Bx | Random Access Area Read Data  | ≥ 4 Bytes (4 bytes wise) |

Figure 24:Acronyms



#### 7.3.1 Write Access

Table 33:: Random Area Write: Remote Command

| Remote Command | Code  | Description       |
|----------------|-------|-------------------|
| RC_RAA_WR[3:0] | b1101 | Random Area Write |

Table 34:: RC\_RAA\_WR (RAA Write in blocks)

| Remote Request  | Answer                         |  |
|-----------------|--------------------------------|--|
| Command Address | RC_RAA_WR[3:0]<br>RAA_ADR[7:4] |  |
| Address         | RAA_ADR[3:0]<br>DUMMY_BIT[3:0] |  |
| Write Data      | RAA_WD0_B3                     |  |
|                 | RAA_WD0_B2                     |  |
|                 | RAA_WD0_B1                     |  |
|                 | RAA_WD0_B0                     |  |
|                 | RAA_WD1_B3                     |  |
|                 | ...                            |  |
|                 | RAA_WDx_B0                     |  |

### 7.3.2 Read Access

Table 35:: Random Area Read: Remote Command

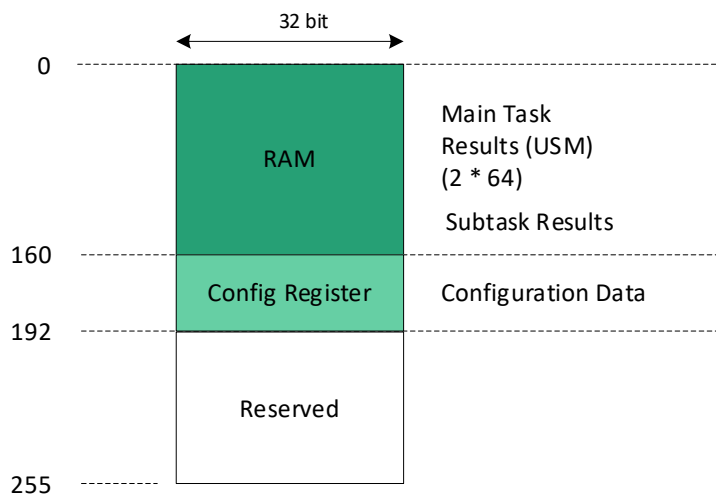
| Remote Command | Code  | Description      |
|----------------|-------|------------------|
| RC_RAA_RD[3:0] | b1110 | Random Area Read |

Table 36:: RC\_RAA\_RD (RAA Read in blocks)

| Remote Request  |                                | Answer    |            |
|-----------------|--------------------------------|-----------|------------|
| Command Address | RC_RAA_RD[3:0]<br>RAA_ADR[7:4] |           |            |
| Address         | RAA_ADR[3:0]<br>DUMMY_BIT[3:0] |           |            |
|                 |                                | Read data | RAA_RD0_B3 |
|                 |                                |           | RAA_RD0_B2 |
|                 |                                |           | RAA_RD0_B1 |
|                 |                                |           | RAA_RD0_B0 |
|                 |                                |           | RAA_RD1_B3 |
|                 |                                |           | ...        |
|                 |                                |           | RAA_RDx_B0 |

### 7.3.3 Random Access Area mapping

Figure 25: RC\_RAA\_RD (RAA Read in blocks)



## 8 RAM Content

The RAM content can be organized in 2 different modes (configured by `C_USM_MHIT_BATCH`):

- **Single Cycle Mode** by providing 1 USM bundle, extendable by up to 61 single TOF results for each direction.
- **Batch Cycle Mode** by providing up to 12 USM bundles.

### 8.1 Single Cycle Mode

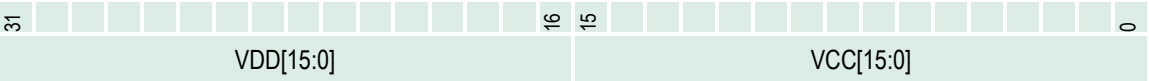
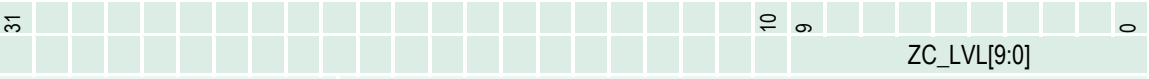
In single cycle mode the complete data for a single flow measurement, including the ToF data, amplitude and pulse width in up and down direction as well as the temperature measurement results and calibration data are stored. It is configured by setting `C_USM_MHIT_BATCH = 0`.

*Table 37: RAM content in single cycle mode*

| Address dec             | Content  | Description   |
|-------------------------|--|---|
| 0 - 11 <sup>11</sup>    | USM Bundle 1   |   |
| 12 - 16                 | Reserved   |   |
| 16 - 76                 | US_TOF_HIT_UP_1[31:0]<br>...<br>US_TOF_HIT_UP_61[31:0] | TOF of the START HIT in up direction<br>...<br>TOF of the 60 <sup>th</sup> hit received after START HIT in up direction |
| 77 - 80                 | Reserved   |   |
| 80 - 140                | US_TOF_HIT_DN_1[31:0]<br>...<br>US_TOF_HIT_DN_61[31:0] | TOF of the START HIT in dn direction<br>...<br>TOF of the 60 <sup>th</sup> hit received after START HIT in dn direction |
| 141 - 143               | Reserved   |   |
| 144 - 153 <sup>11</sup> | Temperature Results                                    |   |
| 154 <sup>11</sup>       | TDC Calibration  | For test & debug purpose only   |
| 155 - 159 <sup>11</sup> | Reserved   |   |

<sup>11</sup> identical to batch cycle mode



| Rel. Bundle Address | Content  | Description   |
|---------------------|--|---|
| + 0x8 (8d)          | VDD[15:0], VCC[15:0]   | Supply measurement value (bits 15 to 10 fixed to 0)                                     |
|                     |  |   |
| + 0x9 (9d)          | HCC_CALIB[31:0]  | High speed oscillator calibration value   |
| + 0xA (10d)         | ZC_LVL[9:0]  | Zero Cross threshold level (either fixed or by calibration).<br>Bit [31:10] set to zero |
|                     |  |   |
| + 0xB (11d)         | Frontend error and status flags  | See detailed definition of dedicated register   |

### 8.3 Batch Cycle Mode

Dependent on configuration of C\_USM\_BATCH\_MODE up to 12 USM bundles can be stored in RAM, but no single TOF hits. It is configured by setting the three bits of C\_USM\_MHIT\_BATCH to select between 1 and maximum 12 bundles (see 9.2.10).

Table 39: RAM content in batch cycle mode

| Address dec | Content                          | Description |
|-------------|----------------------------------|-------------|
| 0 - 11      | USM Bundle 1                     |             |
| 12 - 23     | USM Bundle 2                     |             |
| 24 - 35     | USM Bundle 3                     |             |
| 36 - 47     | USM Bundle 4                     |             |
| 48 - 59     | USM Bundle 5                     |             |
| 60 - 71     | USM Bundle 6                     |             |
| 72 - 83     | USM Bundle 7                     |             |
| 84 - 95     | USM Bundle 8                     |             |
| 96 - 107    | USM Bundle 9                     |             |
| 108 - 119   | USM Bundle 10                    |             |
| 120 - 131   | USM Bundle 11                    |             |
| 132 - 143   | USM Bundle 12                    |             |
| 144 - 159   | As defined for single Batch Mode |             |

## 8.4 Frontend Error and Status Flags

Stored at relative address +0xB

These flags are related to each single batch cycle. They are overwritten by the following run of the same batch cycle.

*Table 40: Error and status flags in +0xB*

| Bit     | Description  |
|---------|--|
| 0       | TDC TO HCC: TDC counter Timeout detected during HCC measurement  |
| 1       | TDC TO TM: TDC counter Timeout detected during temperature measurement   |
| 2       | TM_OPEN: 0 = short on any active TM port, 1 = at least one open error on an active TM port   |
| 3       | TM_SHORT: 0 = no TM error. 1 = TM error, either short or open  |
| 4       | USM HW ERR UP: USM HW error detected in up direction   |
| 5       | USM HW ERR DN: USM HW error detected in down direction   |
| 6       | TDC TO PW UP: TDC counter Timeout detected during Pulse Width measurement in up direction  |
| 7       | TDC TO PW DN: TDC counter Timeout detected during Pulse Width measurement in down direction  |
| 8       | TDC TO TOF UP: TDC counter timeout detected during TOF measurement in up direction   |
| 9       | TDC TO TOF DN: TDC counter timeout detected during TOF measurement in down direction   |
| 10      | USM TO TOF UP: number of expected TOF hits (single or multi) not received before the programmed timeout (defined by C_USM_TMO_SEL) in up direction   |
| 11      | USM TO TOF DN: number of expected TOF hits (single or multi) not received before the programmed timeout (defined by C_USM_TMO_SEL) in down direction |
| 15 - 12 | Not used   |
| 16      | HCC result updated   |
| 17      | ZCC result updated   |
| 18      | VCC/VDD results updated  |
| 19      | Temperature results updated  |
| 20      | USM-UP up sequence done  |
| 21      | USM-DN down sequence done  |
| 31 - 22 | Reserved   |

## 8.5 Temperature results

*Table 41: RAM content in single cycle and batch cycle mode*

| Address dec | Content               | Description             |
|-------------|-----------------------|-------------------------|
| 144         | t <sub>G_s1</sub>     | Gain compensation seq1  |
| 145         | t <sub>Rdson_s1</sub> | RDSON compensation seq1 |
| 146         | t <sub>Ref_s1</sub>   | Reference port seq1     |
| 147         | t <sub>PT1_s1</sub>   | Measure port 1 seq1     |
| 148         | t <sub>PT2_s1</sub>   | Measure port 2 seq1     |
| 149         | t <sub>G_s2</sub>     | Gain compensation seq2  |
| 150         | t <sub>Rdson_s2</sub> | RDSON compensation seq2 |
| 151         | t <sub>Ref_s2</sub>   | Reference port seq2     |
| 152         | t <sub>PT1_s2</sub>   | Measure port 1 seq2     |
| 153         | t <sub>PT2_s2</sub>   | Measure port 2 seq2     |

## 8.6 Result & Status Format within Bundle

### 8.6.1 Amplitude Measurement Results

Stored for 3 configurable waves in up and down direction at relative addresses +0x0 and +0x4 respectively.

Format: 1 LSB = SAR<sub>LSB</sub> ≈ 1.37 mV

### 8.6.2 Pulse Width Measurement Results

Stored for 1<sup>st</sup>, 2<sup>nd</sup> and zero cross hit in up and down direction at relative addresses +0x1/0x2 and +0x5/0x6 respectively.

Format: 1 LSB = PW<sub>LSB</sub>

### 8.6.3 Multi Hit Summation Value

Stored in up and down direction at relative addresses +0x2/0x3 and +0x6/0x7 respectively.

Format: 1 LSB = TOF<sub>LSB</sub>

Effective number of summation depend on TOF\_HIT\_NUM, stored at addresses +0x2(up) and +0x3(dn), bits 15:0.

If TOF\_HIT\_NUM ≥ C\_TOF\_MULTIHIT\_START + C\_TOF\_MULTIHIT\_NO then C\_TOF\_MULTIHIT\_NO are used as programmed for the multi hit summation. Otherwise: TOF\_HIT\_NUM - C\_TOF\_MULTIHIT\_START are used due to timeout error (USM TO TOF error flag is set).

### 8.6.4 Voltage Measurement Results

Stored at relative address +0x8. The effective bit width is 10 Bits. Bits 15-11 are fixed to 0.

VM<sub>STEP\_VCC</sub> for bits [15:0]. 1 LSB = 1.97 \* SAR<sub>LSB</sub> ≈ 2.73 mV

VM<sub>STEP\_VDD</sub> for bits [31:16]. 1 LSB = 2.93 \* SAR<sub>LSB</sub> ≈ 4.1 mV

### 8.6.5 High Speed Calibration Result

Stored at relative address +0x9, fFormat: 1 LSB = T<sub>H50</sub> / 2<sup>16</sup>. Nominal values are:

Table 42: High speed clock calibration nominal values

| f <sub>nom</sub> (TDC_CLK) [MHz] | T <sub>nom</sub> (TDC_CLK) [ns] | HSC_VAL <sub>nom</sub> [dec] | HSC_VAL <sub>nom</sub> [hex] |
|----------------------------------|---------------------------------|------------------------------|------------------------------|
| 4                                | 250                             | 32,000,000                   | 0x01E84800                   |
| 8                                | 125                             | 64,000,000                   | 0x03D09000                   |
| 12                               | 83.33                           | 96,000,000                   | 0x05B8D800                   |
| 16                               | 62.5                            | 128,000,000                  | 0x07A12000                   |

Table 43: High speed clock calibration example

| $f_{nom}(TDC\_CLK)$ [MHz] | $T_{nom}(TDC\_CLK)$ [ns] | HSC_VAL <sub>nom</sub> [dec] | HSC_VAL <sub>nom</sub> [hex] |
|---------------------------|--------------------------|------------------------------|------------------------------|
| 4.000674                  | 249.9579                 | 32,005,389                   | 0x1E85D0D                    |

The correction factor is then:  $32,000,000/32,005,389 = 0.999832$ .

This factor can be used for all further timing calculations in any post processing.

### 8.6.6 Zero Cross Level

Stored at relative addresses +0xA, format: 1 LSB = SAR<sub>LSB</sub> = 1.37 mV.

### 8.6.7 Format of TOF Single Hit Results

Stored for single cycle mode in up and down direction at addresses 0x10...0x4C and 0x50...0x8C respectively.

Format: 1 LSB = TOF<sub>LSB</sub>

Effective number of single hit stored is written in TOF\_HIT\_NUM, stored at addresses +0x2(up) and +0x3(dn), bits 15:0.

### 8.6.8 Format of Temperature Measurement Results

Stored for up to 10 temperature results in address range +0x90...0x99.

Format: 1 LSB = TOF<sub>LSB</sub>

### 8.6.9 Format of TDC calibration

The value of  $4 * T_{HSO}$  is stored on address 0x9A each time a TDC calibration is performed (TOF, HCC or TEMP)

Format: 1 LSB = TDC<sub>LSB</sub>

### 8.6.10 Status

Flags 20 & 21, USM Up Sequence Done & USM Down Sequence Done indicate the end of a sequence. From the configuration the user can extract which measurements are updated (Single hits, multi hits, PWD and AM) and results can be read.

The frontend status flags 16 to 21 are all included in the frontend status flag register which can be read separately by dedicated SPI command.

## 9 Configuration Registers

This section describes the registers of the UFC23 which enable the host system to

- Identify the Device and version information
- Configure the UFC23 and set the operating mode
- Read back STATUS information and the calculated TOF and PW

### 9.1 Register overview

Table 44: Registers Overview

| Address | Name               | Size | Access | Write Access                             |
|---------|--------------------|------|--------|--|
| 0xA0    | CR_FRU_IFH         | 32   | RW     | in STANDBY only                          |
| 0xA1    | CR_FRU_EFH         | 32   | RW     | in STANDBY only                          |
| 0xA2    | CR_GP_CTRL         | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xA3    | CR_PM              | 32   | RW     | in STANDBY only, LF domain               |
| 0xA4    | CR_TSC             | 32   | RW     | in STANDBY and MEAS_IDLE only, LF domain |
| 0xA5    | CR_MCT             | 32   | RW     | in STANDBY only, LF domain               |
| 0xA6    | CR_MRG             | 32   | RW     | in STANDBY and MEAS_IDLE only, LF domain |
| 0xA7    | CR_FEP_MCTRL       | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xA8    | <i>Reserved</i>    |      |        |  |
| 0xA9    | CR_FEP_TDC_TRIM    | 32   | RW     | in STANDBY only                          |
| 0xAA    | CR_USM_PROC        | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xAB    | CR_USM_FBG_MCTRL   | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xAC    | <i>Reserved</i>    | 32   | RW     |  |
| 0xAD    | CR_ANALOG_CTRL1    | 32   | RW     | in STANDBY only                          |
| 0xAE    | CR_ANALOG_CTRL2    | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xAF    | CR_USM_RCV_INIT    | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xB0    | CR_USM_HIT_CTRL    | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xB1    | CR_USM_WVM         | 32   | RW     | in STANDBY and MEAS_IDLE only            |
| 0xB2    | CR_USM_MASK_HR_WIN | 32   | RW     | in STANDBY and MEAS_IDLE only            |

All system relevant parameter are stored in configuration register which can be accessed via system bus by SPI Sub controller only (write & read access).

Write access for updating configuration registers is not enabled all the time. Following update modes can be distinguished

- **Initial Update:**  
As long device is in STANDBY state, all configuration register can be written arbitrarily.
- **Cyclic Update:**  
When the device is in MEAS/MEAS\_IDLE state, some registers can't be updated, some affect the LF domain and request 4 LF cycles between to write commands. All other config register can be updated by releasing SPI access during MEAS\_IDLE

## 9.2 Detailed register description

### 9.2.1 CR\_FRU\_IFH (Interrupt Flag Handling) (Address 0xA0)

Table 45: CR\_FRU\_IFH Interrupt flags

| Bit  | Description  | Recom <sup>13</sup> . | Default |
|------|--|-----------------------|---------|
| 0    | <b>C_IRQ_EN_BL_DONE:</b> Interrupt Request Enable, Bootload Done   | 1                     | 1       |
| 1    | <b>C_IRQ_EN_MIS_DONE:</b> Interrupt Request Enable, Measure Init Done  | 1                     | 1       |
| 2    | <b>C_IRQ_EN_MCS_DONE:</b> Interrupt Request Enable, Measure Cycle Done<br>Single cycle mode<br>Batch cycle mode                | 1                     | 1       |
|      |  | 0                     |         |
| 3    | <b>C_IRQ_EN_MC_BATCH_DONE:</b> Interrupt Request Enable, Batch of Measure Cycle Done.<br>Single cycle mode<br>Batch cycle mode | 1                     | 1       |
|      |  | 1                     |         |
| 4    | <b>C_IRQ_EN_STASK_DONE:</b> Interrupt Request Enable, Service Task Done  | 1                     | 1       |
| 5    | <b>C_IRQ_EN_USM_PAUSE_ERR:</b> Interrupt Request Enable, Ultrasonic Measurement Pause Error                                    | 1                     | 1       |
| 6    | <b>C_IRQ_EN_TSC_TMO:</b> Interrupt Request Enable, Task Sequencer Timeout  | 1                     | 1       |
| 31:7 | <i>Reserved</i>  | 0                     | 0       |

<sup>13</sup> Recom. = recommended

### 9.2.2 CR\_FRU\_EFH (Error Flag Handling) (Address 0xA1)

Table 46: CR\_FRU\_EFH Error flag handling

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 0     | <b>C_EF_EN_HCC_TDC_TMO</b> : Error Flag Enable, HCC TDC Timeout             | 1      | 0       |
| 1     | <b>C_EF_EN_TM_TDC_TMO</b> : Error Flag Enable, TM TDC Timeout               | 1      | 0       |
| 2     | <b>C_EF_EN_TM_ERR</b> : Error Flag Enable, TM Open circuit or short circuit | 1      | 0       |
| 3     |   | 1      | 0       |
| 4     | <b>C_EF_EN_USM_HW_UP_ERR</b> : Error Flag Enable, USM HW Error Up           | 1      | 0       |
| 5     | <b>C_EF_EN_USM_HW_DN_ERR</b> : Error Flag Enable, USM HW Error Dn           | 1      | 0       |
| 6     | <b>C_EF_EN_PW_UP_TDC_TMO</b> : Error Flag Enable, PW TDC Timeout Up         | 1      | 0       |
| 7     | <b>C_EF_EN_PW_DN_TDC_TMO</b> : Error Flag Enable, PW TDC Timeout Dn         | 1      | 0       |
| 8     | <b>C_EF_EN_TOF_UP_TDC_TMO</b> : Error Flag Enable, TOF TDC Timeout Up       | 1      | 0       |
| 9     | <b>C_EF_EN_TOF_DN_TDC_TMO</b> : Error Flag Enable, TOF TDC Timeout Dn       | 1      | 0       |
| 10    | <b>C_EF_EN_USM_UP_TMO</b> : Error Flag Enable, USM Timeout Up               | 1      | 0       |
| 11    | <b>C_EF_EN_USM_DN_TMO</b> : Error Flag Enable, USM Timeout Dn               | 1      | 0       |
| 31-12 | <i>Reserved</i>   | 0      | 0       |

### 9.2.3 CR\_GP\_CTRL (General Purpose Control) (Address 0xA2)

Table 47: CR\_GP\_CTRL general purpose IO control

| Bit   | Description                                  | Recom. | Default |
|-------|--|--------|---------|
| 2-0   | <b>C_GPIO0_MODE</b> : For test purposes only | 3      | 3       |
| 5-3   | <b>C_GPIO1_MODE</b> : For test purposes only | 3      | 3       |
| 8-6   | <b>C_GPIO2_MODE</b> : For test purposes only | 3      | 3       |
| 11-9  | <b>C_GPIO3_MODE</b> : For test purposes only | 3      | 3       |
| 31-12 | <i>Reserved</i>                              | 0      | 0       |

### 9.2.4 CR\_PM (Power Management) (Address 0xA3)

Table 48: CR\_PM Power management

| Bit  | Description   | Recom.     | Default |
|------|---|------------|---------|
| 2:0  | <b>C_LDO_RF_RATE:</b> LDO refresh rate state<br>000: 64 Hz<br>001: 32 Hz<br>010: 16 Hz<br>011: 8 Hz<br>100: 4 Hz<br>101: 2 Hz<br>110: 1 Hz<br>111: 0.5 Hz | 3<br>(8Hz) | 0       |
| 3    | Reserved  | 0          | 0       |
| 4    | Reserved  | 1          | 1       |
| 31:5 | Reserved  | 0          | 0       |

This register is transferred into the LF clock domain so the latency time between 2 consecutive write at this address is 4 LF clock cycles , in case of latency violation the second write is ignored.

### 9.2.5 CR\_TSC (Task Sequence Control) (Address 0xA4)

Table 49: CR\_TSC Task sequence control

| Bit | Description   | Recom. | Default |
|-----|---|--------|---------|
| 2:0 | <b>C_USM_PAUSE_TSEL:</b> Pause time between 2 US measurements up-dn (multiple of LS period)<br>000: Pause time ≈ 0.5 ms<br>001: Pause time ≈ 1 ms<br>010: Pause time ≈ 2 ms<br>011: Pause time ≈ 4 ms<br>100: Pause time ≈ 8 ms<br>101: Pause time ≈ 10 ms<br>110: Pause time ≈ 16.66 ms<br>111: Pause time ≈ 20 ms |        | 7       |
| 3   | <b>C_USM_REPEAT:</b> Ultrasonic Measurement Repeat Mode<br>0: Only 1 ultrasonic measurement performed<br>1: 2 US measurements performed in different directions, separated by pause time  |        | 1       |
| 5:4 | <b>C_USM_DIR_MODE:</b> Ultrasonic Measurement Direction Mode<br>1x: Toggling direction with every US measurement  | 2      | 2       |

|       |   |   |   |
|-------|---|---|---|
| 7:6   | <b>C_USM_EDGE_MODE:</b> USM TOF Measurement, Edge Mode<br>00: TOF measurement on positive edge of TOF Hit, standard setting<br>01: TOF measurement on negative edge of TOF Hit<br>10: Edge for TOF measurement toggling after every measurement cycle<br>11: Edge for TOF measurement toggling after every 2. measurement cycle | 0 | 2 |
| 9:8   | <b>C_LDO_STUP_TSEL:</b> LDO Startup Timing Select (multiple of LS period)<br>00: ~0.25 ms<br>01: ~0.5 ms<br>10: ~1.0 ms<br>11: ~2.0 ms  | 3 | 1 |
| 10    | <b>C_LDO_FEP_MODE:</b> LDO request by task sequencer during frontend processing (by signal LDO_REQ_TSC)<br>0: LDO not requested during frontend processing<br>1: LDO requested during frontend processing   | 1 | 1 |
| 12:11 | <b>C_TM_SQC_MODE:</b> Temperature Measurement Sequence Mode<br>10: Toggling order with every TM measurement   | 2 | 2 |
| 31:13 | <i>Reserved</i>   | 0 | 0 |

This register is transferred into the LF clock domain, so the latency time between 2 consecutive write at this address is 4 LF clock cycles, in case of latency violation the second write is ignored.

### 9.2.6 CR\_MCT (Measure Cycle Timer) (Address 0xA5)

Table 50: CR\_MCT Measure cycle timer

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 11:0  | <b>C_MCYCLE_TIME:</b> Measure Cycle Time (Unsigned integer), generates Measure Cycle Trigger, format UINT<br>0 - 9: Measure Cycle Time = 9765.625 $\mu$ s<br>10 - 4095: Measure Cycle Time = C_MCYCLE_TIME * 976.5625 $\mu$ s   |        | 128     |
| 14:12 | <b>C_MCYCLE_TAIL_SEL:</b> Measure Cycle, Tail Time Select, can be used to estimate the remaining time available for communication<br>000: ~ 488 $\mu$ s<br>001: ~ 977 $\mu$ s<br>010: ~ 1.465 ms<br>011: ~ 1.953 ms (default)<br>100: ~ 2.930 ms<br>101: ~ 3.910 ms<br>110: ~ 5.859 ms<br>111: ~ 7.813 ms |        | 3       |

|       |  |   |   |
|-------|--|---|---|
| 15    | <b>C_MCT_EN:</b> Measure Cycle Timer Enable<br>0: MCT Disabled<br>1: MCT Enabled |   | 0 |
| 31:16 | <i>Reserved</i>  | 0 | 0 |

This register is transferred into the LF clock domain, so the latency time between 2 consecutive write at this address is 4 LF clock cycles, in case of latency violation the second write is ignored.

### 9.2.7 CR\_MRG (Measure Rate Generator) (Address 0xA6)

Table 51: CR\_MRG Measure rate generator

| Bit  | Description  | Recom. | Default |
|------|--|--------|---------|
| 2:0  | <b>C_USM_RATE:</b> Ultrasonic Measurement Rate<br>000: US measurement not triggered by MCT<br>001: US measurement every measure cycle trigger<br>010: US measurement every 2. measure cycle trigger<br>011: US measurement every 4. measure cycle trigger<br>1xx: US measurement every 8. measure cycle trigger  |        | 1       |
| 5:3  | <b>C_ZCC_RATE:</b> Zero Cross Calibration Rate<br>000: Zero cross calibration not triggered by MCT<br>001: Zero cross calibration every measure cycle trigger<br>010: Zero cross calibration every 2. measure cycle trigger<br>011: Zero cross calibration every 4. measure cycle trigger<br>100: Zero cross calibration every 8. measure cycle trigger<br>101: Zero cross calibration every 16. measure cycle trigger<br>110: Zero cross calibration every 32. measure cycle trigger<br>111: Zero cross calibration every 64. measure cycle trigger<br><br>(shall be < than C_USM_RATE) | 7      | 3       |
| 8:6  | <b>C_VM_RATE:</b> VCC/VDD Measurement Rate<br>000: VCC Measurement not triggered by MCT<br>001: VCC Measurement every measure cycle trigger<br>010: VCC Measurement every 2. measure cycle trigger<br>011: VCC Measurement every 4. measure cycle trigger<br>100: VCC Measurement every 8. measure cycle trigger<br>101: VCC Measurement every 16. measure cycle trigger<br>110: VCC Measurement every 32. measure cycle trigger<br>111: VCC Measurement every 64. measure cycle trigger<br><br>(shall be < than C_USM_RATE)   |        | 1       |
| 11:9 | <b>C_HCC_RATE:</b> High-Speed Clock Calibration Rate<br>000: HS Clock Calibration not triggered by MCT<br>001: HS Clock Calibration every measure cycle trigger<br>010: HS Clock Calibration every 2. measure cycle trigger<br>011: HS Clock Calibration every 4. measure cycle trigger<br>100: HS Clock Calibration every 8. measure cycle trigger  | 7      | 3       |

|       |   |   |   |
|-------|---|---|---|
|       | 101: HS Clock Calibration every 16. measure cycle trigger<br>110: HS Clock Calibration every 32. measure cycle trigger<br>111: HS Clock Calibration every 64. measure cycle trigger<br>(shall be < than C_USM_RATE) |   |   |
| 15:12 | <i>Reserved</i>   | 0 | 0 |
| 25:16 | <b>C_TM_RATE:</b> Temperature Measurement Rate, format UINT<br>0: Temperature measurement disabled<br>1...1023: Performed by every configured measure cycle trigger (shall be < than C_USM_RATE)                    |   | 0 |
| 31:26 | <i>Reserved</i>   | 0 | 0 |

This register is transferred into the LF clock domain, so the latency time between 2 consecutive write at this address is 4 LF clock cycles, in case of latency violation the second write is ignored.

### 9.2.8 CR\_FEP\_MCTRL (Front End Control) (Address 0xA7)

Table 52: CR\_FEP\_MCTRL Front end control

| Bit  | Description  | Recom. | Default |
|------|--|--------|---------|
| 2:0  | <b>C_FEP_4M_CLK_DIV:</b> Selects division factor to get an internal 4 MHz clock from external provided HSO clock. This internal generated 4 MHz clock is then provided to dedicated frontend timers (e.g. for noise mask window)<br><br>000: undefined / not calculated<br>001: 4 MHz<br>010: 8 MHz<br>011: 12 MHz<br>100: 16 MHz<br>101: 20 MHz (default)<br>110/111: undefined |        | 5       |
| 3    | <b>C_ADC_ST:</b> ADC Step Width<br>0: 1,0 μs   | 0      | 0       |
| 7:4  | <b>C_FEP_STUP_TSEL:</b> Time until any FEP measurement gets released (HSO settling time for accurate TDC measurement)<br><br>0000-1011: 40 + (C_FEP_STUP_TSEL * 10) us<br>1100: 200 us<br>1101: 250 us<br>1110: 350 us<br>1111: 500 us<br>f(FEP_SQC_CLK) = 1 MHz   |        | 8       |
| 11:8 | <b>C_USM_TMO_SEL:</b> Timeout Ultrasonic Measurement<br>0000: No timeout<br>0001: 256*T_HSO (64 us @ 4M)   |        | 3       |

|       |   |   |   |
|-------|---|---|---|
|       | 0010: 512*T_HSO (128 us @ 4M)<br>0011: 1024*T_HSO (256 us @ 4M, default)<br>0100: 2048*T_HSO (512 us @ 4M)<br>0101: 2560*T_HSO (640 us @ 4M)<br>0110: 3072*T_HSO (768 us @ 4M)<br>0111: 3584*T_HSO (896 us @ 4M)<br>1000: 4096*T_HSO (1024 us @ 4M)<br>1001: 6144*T_HSO (1536 us @ 4M)<br>1010: 8192*T_HSO (2048 us @ 4M)<br>1011: 10240*T_HSO (2560 us @ 4M)<br>1100: 12288*T_HSO (3072 us @ 4M)<br>1101: 16384*T_HSO (4096 us @ 4M)<br>1110: 32768*T_HSO (8192 us @ 4M)<br>1111: 65536*T_HSO (16384 us @ 4M)<br>The timeout starts with the sequence of the fire burst. It has to be selected to a value which covers fire burst sequence, time of flight and receive burst sequence. |   |   |
| 12    | <b>C_TM_PORT_NO:</b> Temperature Measurement Port Number<br>0: 1port<br>1: 2 ports  |   | 0 |
| 13    | <b>C_TM_PORT_MODE:</b> Temperature Measurement Port Mode<br>0: Inactive ports pulled to GND while measurement<br>1: Inactive ports set to HighZ while measurement   |   | 0 |
| 15:14 | <b>C_TM_CYCLE_SEL:</b> Temperature Measurement Cycle Select<br>00: 256 us (speed up option 1)<br>01: 384 us (speed up option 2)<br>10: 512 us (default, recommended for typical application)<br>11: 1024 us (slow down option for production test)  |   | 2 |
| 16    | <b>C_TM_SQC_NO:</b> Temperature Measurement Sequence Number<br>0: 1 sequence<br>1: 2 sequences in reversed order  |   | 0 |
| 31:17 | <i>Reserved</i>   | 0 | 0 |

9.2.9 Reserved (Address 0xA9)

Table 53: Reserved

| Bit   | Description     | Recom. | Default |
|-------|-----------------|--------|---------|
| 15:0  | <i>Reserved</i> | 0x0000 | 0x0000  |
| 31:16 | <i>Reserved</i> | 0x0490 | 0x0490  |

### 9.2.10 CR\_USM\_PROC (Ultrasonic Processing) (Address 0xAA)

Table 54: CR\_USM\_PROC Ultrasonic processing

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 12:0  | <b>C_USM_MASK_WIN:</b> Mask window before ultrasonic receive burst gets released, format UINT<br>1 LSB: 1 $\mu$ s, an offset of 1 to 2 $\mu$ s will be added<br>Minimum value: 2<br>Maximum value: 8191   |        | 2       |
| 15:13 | <b>C_USM_MHIT_BATCH:</b> Number US Multi Hits per batch<br><br>000: Single cycle mode: 1 USM bundle<br>001: Batch cycle mode: 2 USM bundles<br>010: Batch cycle mode: 4 USM bundles<br>011: Batch cycle mode: 6 USM bundles<br>100: Batch cycle mode: 8 USM bundles<br>101: Batch cycle mode: 10 USM bundles<br>11x: Batch cycle mode: 12 USM bundles |        | 0       |
| 16    | <b>C_USM_SENSOR_MODE:</b> Ultrasonic Sensor Mode<br>0: 1 Sensor only (sending & receiving on same transducer)<br>1: 2 Sensor (sending & receiving by 2 opposite transducer)   |        | 1       |
| 17    | <b>C_USM_AM_MODE:</b> Amplitude Measurement Mode<br>0: Cyclic Amplitude Measurement disabled<br>1: Cyclic Amplitude Measurement enabled   |        | 0       |
| 19:18 | <b>C_USM_PWD_MODE:</b> Pulse Width Detection Mode<br>0x: Cyclic pulse width only for 1 <sup>st</sup> hit<br>10: Cyclic pulse width detection enabled: 1 FHL PW and 1 ZCL PW<br>11: Cyclic double pulse width detection enabled: 2 FHL PW and 1 ZCL PW   |        | 2       |
| 29:20 | <b>C_ZCD_LVL:</b> Zero Cross Detection Level, format UINT<br>Zero cross calibration disabled (C_ZCC_MODE = b0): Writing constant value for zero cross level<br>Zero cross calibration enabled (C_ZCC_MODE = b1): Ignored  |        | 0       |
| 30    | <b>C_ZCC_MODE:</b> Zero Cross Calibration Mode<br>0: C_ADC_ZCD_LVL provided without calibration<br>1: SAR algorithm   |        | 1       |
| 31    | <b>C_ZCC_INIT_EN:</b> Zero Cross Calibration...<br>0: not performed during measure init sequence<br>1: performed during measure init sequence   |        | 1       |

### 9.2.11 CR\_USM\_FBG\_MCTRL (Fire Burst Generator Control) (Address 0xAB)

Table 55: CR\_USM\_FBG\_MCTRL Fire burst generator control

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 0     | Reserved, set 0   | 0      | 0       |
| 6:1   | <b>C_FBG_LR_CLK_DIV:</b> Fire burst generator clock divider, format UINT<br>0: not allowed<br>1-63: High speed clock divided by 4//6/.../124/126/128<br>$f_{Fire} => f_{FEP\_CLK} / (2*(C\_FPG\_LR\_CLK\_DIV+1))$<br>$f_{Fire}$ : Fire frequency $f_{FEP\_CLK}$ : FEP Clock frequency |        | 1       |
| 12:7  | <b>C_FBG_FBNUM:</b> number of fire burst pulse, format UINT<br>0: not allowed<br>1-63: 1-63 pulses  |        | 10      |
| 18:13 | <b>C_FBG_FBSP:</b> Selection fire burst pulse for fire burst splitting.<br>0: Fire burst split not enabled<br>1 to 63: Selected pulse   |        | 0       |
| 21:19 | <b>C_FSPLITWID:</b> Split width in quarter periods.<br>000: $T_{split} = 1*T_{burst}/4$<br>001: $T_{split} = 2*T_{burst}/4$<br>010: $T_{split} = 3*T_{burst}/4$<br>...<br>111: $T_{split} = 8*T_{burst}/4$  |        | 0       |
| 31:22 | Reserved  | 0      | 0       |

### 9.2.12 Reserved (Address 0xAC)

Table 56: Reserved

| Bit  | Description | Recom. | Default |
|------|-------------|--------|---------|
| 31:0 | Reserved    | 0      | 0       |

### 9.2.13 CR\_ANALOG\_CTRL1 (Analog Control) (Address 0xAD)

Table 57: CR\_ANALOG\_CTRL1 Ultrasonic frontend analog control

| Bit   | Description | Recom  | Default |
|-------|-------------|--------|---------|
| 15:0  | Reserved,   | 0xB00F | 0x0000  |
| 31:16 | Reserved    | 0x0C08 | 0x0800  |

### 9.2.14 CR\_ANALOG\_CTRL2 (Analog Control) (Address 0xAE)

Table 58: CR\_ANALOG\_CTRL2 Ultrasonic frontend analog control

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 1:0   | <b>C_PGA_ST2_GAIN:</b> PGA2 Gain selection  |        | 0       |
| 2     | <b>C_PGA_ST2_CBYP:</b> Enables gate that bypass PGA stage 2<br>0: PGA stage 2 not bypassed<br>1: PGA stage 2 bypassed                               |        | 0       |
| 7:3   | <b>C_PGA_ST1_GAIN:</b> PGA1 Gain selection  |        | 0       |
| 8     | <b>C_PGA_ST1_CBYP:</b> Enables gate that bypass PGA stage 1<br>0: PGA stage 1 not bypassed<br>1: PGA stage 1 bypassed                               |        | 0       |
| 9     | <b>C_PGA_G1_OPEN:</b> Unity gain configuration for PGA stage 1<br>0: Default gain configuration, capacitor connected<br>1: Unity gain configuration |        | 0       |
| 11:10 | <i>Reserved</i>   |        | 0       |
| 12    | <b>C_PGA_ST1_OPAN_ENA:</b> PGA 1 <sup>st</sup> stage enable (inverting input)   |        | 0       |
| 13    | <b>C_PGA_ST1_OPAP_ENA :</b> PGA 1 <sup>st</sup> stage enable (non-inverting input)  |        | 0       |
| 14    | <b>C_PGA_ST2_OPA_ENA:</b> PGA 2 <sup>nd</sup> stage enable  |        | 0       |
| 19:15 | <i>Reserved</i>   |        | 0       |
| 24:20 | <b>C_RMSET_RX:</b> RX Resistor Matching Setting, see Table 9  |        | 0       |
| 29:25 | <b>C_RMSET_TX:</b> TX Resistor Matching Setting, see Table 9  |        | 0       |
| 30    | <b>C_SE_ENABLE:</b> Enables single ended (water system)   |        | 0       |
| 31    | <i>Reserved</i>   |        | 0       |

### 9.2.15 CR\_USM\_RCV\_INIT (Ultrasonic Receiver Initialization) (Address 0xAF)

Table 59: 9.2.13 CR\_USM\_RCV\_INIT Ultrasonic receiver initialization

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 7:0   | <b>C_US_VR_INIT:</b> US Vref Init Time in us  | 85     | 0       |
| 13:8  | <b>C_PGA_INIT:</b> PGA Init Time in us  | > 15   | 0       |
| 15:14 | <b>C_COMP_INIT :</b> RX comparator Init Time in us  | 3      | 0       |
| 20:16 | <b>C_ADC_VR_INIT:</b> ADC Vref Init Time in us  | >10    | 0       |
| 23:21 | <b>C_ADC_INIT:</b> ADC Init Time in us  | 7      | 0       |
| 25:24 | <b>C_USM_INIT_MODE:</b> Ultrasonic Measurement Initialization Mode<br>00: USVREF/PGA/ADC initialization directly before receiving is released<br>01: USVREF initialization directly before transmitting fire burst.PGA/ADC initialization directly before receiving is released<br>10: USVREF / PGA initialization directly before transmitting fire burst. ADC initialization directly before receiving is released<br>11: USVREF/PGA/ADC initialization directly before transmitting fire burst | 3      | 3       |
| 31:26 | <i>Reserved</i>   | 0      | 0       |

For C\_USM\_INIT\_MODE the setting b11 is recommended. This sets conditions also for some other parameters to get a correct operation:

- C\_ADC\_INIT between 0  $\mu$ s and 7  $\mu$ s, 7  $\mu$ s recommended
- C\_ADC\_VR\_INIT between 0  $\mu$ s and 31  $\mu$ s, > 10  $\mu$ s recommended
- C\_COMP\_INIT between 0  $\mu$ s and 3  $\mu$ s, 3  $\mu$ s recommended
- C\_PGA\_INIT between 0  $\mu$ s and smaller than C\_FEP\_STUP\_TSEL (reg 0xA7 bit 7..4)  $\geq$  15  $\mu$ s recommended
- C\_US\_VR\_INIT between 85  $\mu$ s and smaller than C\_FEP\_STUP\_TSEL (reg 0xA7 bit 7..4)

C\_COMP\_INIT, CR\_ADC\_VR\_INIT, CR\_ADC\_INIT need not be active during fire burst.

Note: In single transducer mode (C\_USM\_SENSOR\_MODE = 0) C\_USM\_INIT\_MODE has to be set b01!

### 9.2.16 CR\_USM\_HIT\_CTRL (Ultrasonic Hit Control) (Address 0xB0)

Table 60: 9.2.14 CR\_USM\_HIT\_CTRL Ultrasonic hit control

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 5:0   | <b>C_TOF_HIT_NO:</b> Number of TOF hits stored in RAM (counting from START hit), format UINT<br>0: No single hit stored<br>1: START HIT stored<br>2: START HIT + 1 following stored<br>...<br>61: START HIT + 60 following stored<br><br>As the START hit depends on the PWM_MODE and the maximum number of received hits is 63 the maximum hits in RAM are 61 in PWM_MODE 0/1, 60 in PWM_MODE 2 and 59 in PWM_MODE 3 |        | 1       |
| 6     | <b>C_TOF_HIT_RLS_MODE:</b> TOF Hit Release Mode<br>0: Hit release condition derived from First Hit Level Detection only<br>1: Hit release condition derived from USM_HIT_RLS_DLY_U/D  |        | 0       |
| 7     | <b>C_TOF_HIT_IGN_MODE:</b> TOF Hit Ignore Mode<br>0: No TOF Hits ignored<br>1: Ignores every 2 <sup>nd</sup> TOF Hit. TOF_HIT_NO is limited then to 30  | 0      | 0       |
| 12:8  | <b>C_TOF_MULTIHIT_START:</b> Number of TOF hits from START HIT (after comparator offset switched from FHL to ZC and eventual Pulse width detection) before starting multi-hit summation (see C_TOF_MULTIHIT_NO), format uint<br>0: 0 Hits (START HIT)<br>1: 1 Hits (START_HIT + 1)<br>2: 2 Hits (START_HIT + 2)<br>...<br>31: 31 Hits (START_HIT + 31)  |        | 2       |
| 17:13 | <b>C_TOF_MULTIHIT_NO:</b> Number of TOF hits taken for multi-hit summation; format UINT<br>0: No multi-hit storage<br>1: 1 Hit (no summation)<br>2: 2 Hits<br>...<br>31: 31 Hits  |        | 1       |
| 31:18 | Reserved  | 0      | 0       |

START\_HIT = 3 (PWM\_MODE<2), = 4 (PWM\_MODE=2), = 5 (PWM\_MODE=3)

START\_HIT + C\_TOF\_MULTIHIT\_START+ C\_TOF\_MULTIHIT\_NO < 64

START\_HIT + C\_TOF\_HIT\_NO - 1 < 64 (-1 because C\_TOF\_HIT\_NUMBER = 1 means start hit only)

### 9.2.17 CR\_USM\_WVM (ultrasonic Wave Monitor) (Address 0xB1)

Table 61: 9.2.15 CR\_USM\_WVM Ultrasonic wave monitor

| Bit   | Description   | Recom. | Default |
|-------|---|--------|---------|
| 7:0   | <b>C_USM_FHL_UP</b> : US Measurement, First Hit Level Up, format UINT<br>1 LSB = 1.37 mV, added to USVREF (~700mV)  |        | 0       |
| 15:8  | <b>C_USM_FHL_DN</b> : US Measurement, First Hit Level Down<br>1 LSB = 1.37 mV, added to USVREF (~700mV)   |        | 0       |
| 20:16 | <b>C_USM_AM_PD_1</b> : Amplitude Monitoring, Measure peak 1, format UINT<br>Number of hits until peak detection ends<br>0: not allowed<br>1: 1 Hit (First Hit)<br>2: 2 Hits<br>...<br>29: 29 Hits |        | 1       |
| 25:21 | <b>C_USM_AM_PD_2</b> : Amplitude Monitoring, Measure peak 2<br>Number of hits until peak detection ends, format UINT<br>0: not allowed<br>1: 1 Hit (First Hit)<br>2: 2 Hits<br>...<br>30: 30 Hits |        | 2       |
| 30:26 | <b>C_USM_AM_PD_3</b> : Amplitude Monitoring, Measure peak 3<br>Number of hits until peak detection ends, format UINT<br>0: not allowed<br>1: 1 Hit (First Hit)<br>2: 2 Hits<br>...<br>31: 31 Hits |        | 8       |
| 31    | <i>Reserved</i>   | 0      | 0       |

### 9.2.18 CR\_USM\_MASK\_HR\_WIN (High resolution receiver mask in up direction) (Address 0xB2)

Table 62: 9.2.16 CR\_USM\_MASK\_HR\_WIN High resolution receiver mask

| Bit   | Description  | Recom. | Default |
|-------|--|--------|---------|
| 15:0  | <b>C_USM_MASK_HR_WIN_UP:</b><br>High resolution mask window in up direction, after which TOF hits are released. Starting time of delay window refers to rising edge of 1 <sup>st</sup> fire pulse, format UINT<br>1 LSB: T_HS_OSC, an offset of 4 LSB is added<br>The use of this window can be activated by C_TOF_HIT_RLS_MODE.   |        | 0       |
| 31:16 | <b>C_USM_MASK_HR_WIN_DN:</b><br>High resolution mask window in dn direction, after which TOF hits are released. Starting time of delay window refers to rising edge of 1 <sup>st</sup> fire pulse, format UINT<br>1 LSB: T_HS_OSC, , an offset of 4 LSB is added<br>The use of this window can be activated by C_TOF_HIT_RLS_MODE. |        | 0       |

## 9.3 Reference Configuration

Single-ended water meter with 52 $\mu$ s time-of-flight, 2 MHz transducers.

|                  |   |
|------------------|---|
| 0x00000067, //A0 | for single cycle mode, for batch cycle mode 0x6B                                  |
| 0x00000FFF, //A1 |   |
| 0x000006DB, //A2 |   |
| 0x00000013, //A3 | LDO refresh rate 8 Hz   |
| 0x0000172f, //A4 | 20ms between up and down, 2ms LDO setup time                                      |
| 0x0000B080, //A5 | Measure cycle time 128 = 8Hz  |
| 0x00000E79, //A6 |   |
| 0x000198E4, //A7 | 350 $\mu$ s settling time   |
| 0x00000000, //A8 |   |
| 0x04900000, //A9 |   |
| 0xC00F0028, //AA | TOF mask window 40 $\mu$ s  |
| 0x00000B06, //AB | 2 MHz fire frequency, 22 pulses   |
| 0x00000000, //AC |   |
| 0x0C08B00F, //AD |   |
| 0x4A501004, //AE | PGA1 with gain 2, PGA2 bypassed, resistors TX and RX = 5 (162 Ohm)                |
| 0x03EACF55, //AF | USM_INIT_MODE = 3   |
| 0x00014410, //B0 | Start hit 4, 10 hits, 16 hits stored  |
| 0x20411414, //B1 | Amplitude on 1 <sup>st</sup> , 2 <sup>nd</sup> and 8 <sup>th</sup> wave, FHL 27mV |
| 0x00000000 //B2  | No high-resolution mask window, FHL detection only                                |

# 10 Application Information

## 10.1 Schematic

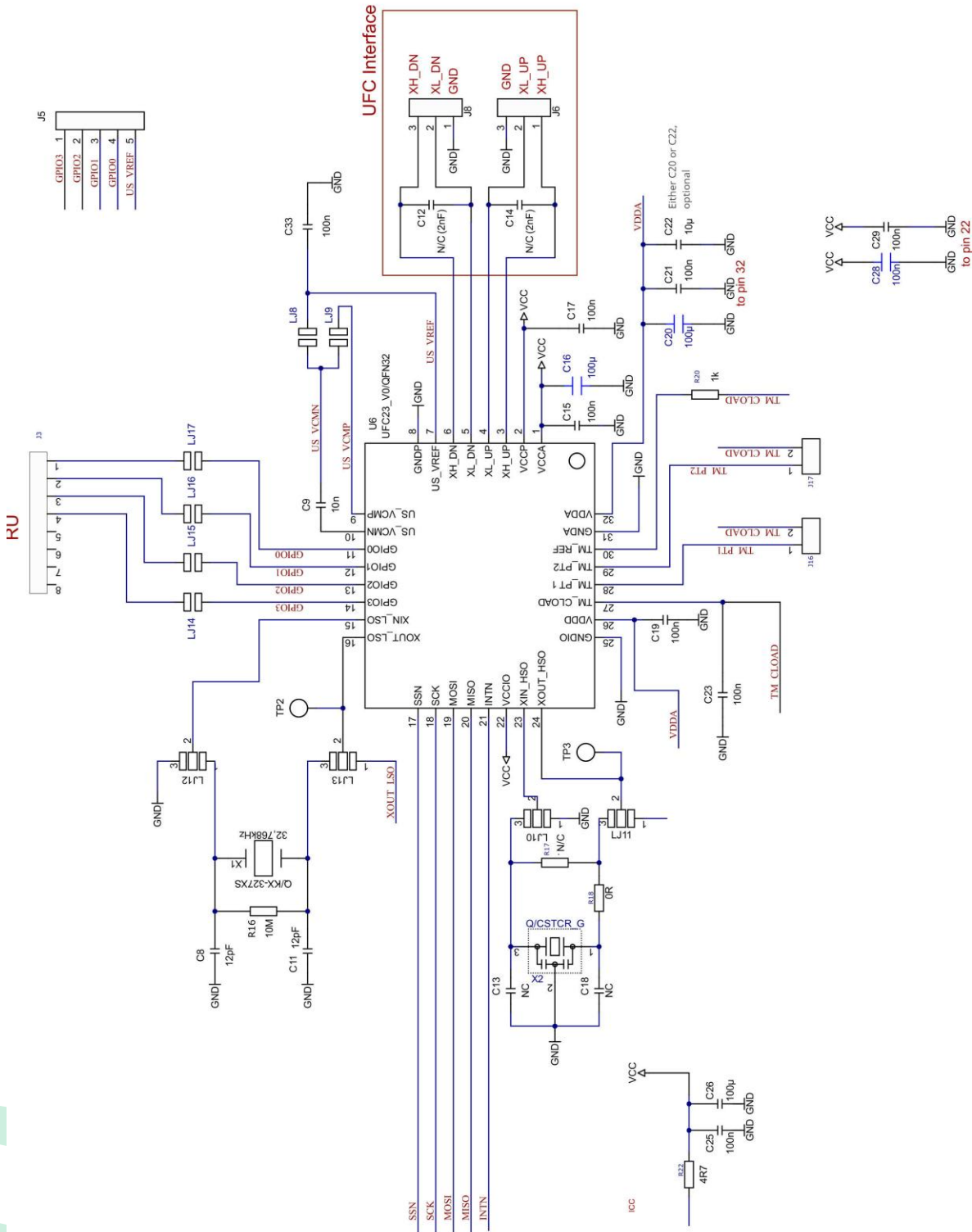


Figure 26: UFC demo board schematics

## 10.2 Code Examples

Code examples for UFC are available from the GitHub platform:

<https://github.com/search?q=org%3Asciosense%20UFC&type=repositories>

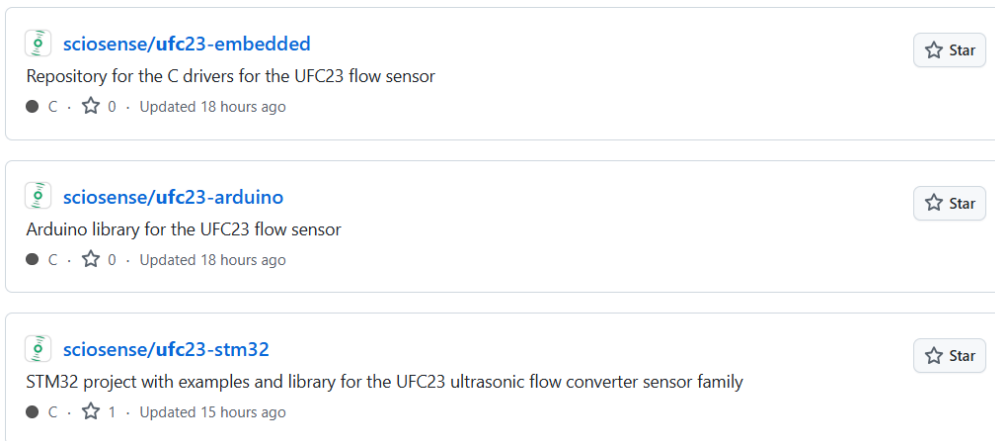


Figure 27: GitHub

There we offer examples to read single values, batches, to run low power and ultra-low power mode, to have split burst and a simple linear flow calculation with filtering.

| ufc23-stm32 / UFC23_Sample_Code / Core / Src / SciSense / |  |
|---|--|
| ..  |  |
| src   | Added split burst and flow calculation examples. Added filter for flow   |
| 01_Basic.cpp  | Added split burst and flow calculation examples. Added filter for flow   |
| 02_Batch.cpp  | Added split burst and flow calculation examples. Added filter for flow   |
| 03_Signal_Values.cpp                                      | Corrected HCC correction factor usage, added PGA gain scaling to ampl... |
| 04_Individual_Hits.cpp                                    | Added split burst and flow calculation examples. Added filter for flow   |
| 05_Temperature.cpp  | Added split burst and flow calculation examples. Added filter for flow   |
| 06_Gas.cpp  | Added split burst and flow calculation examples. Added filter for flow   |
| 07_Low_Power_Mode.cpp                                     | Corrected HCC correction factor usage, added PGA gain scaling to ampl... |
| 08_Ultra_Low_Power_Mode.cpp                               | Corrected HCC correction factor usage, added PGA gain scaling to ampl... |
| 09_Split_Burst.cpp  | Added split burst and flow calculation examples. Added filter for flow   |
| 10_Flow_Conversion.cpp                                    | Added split burst and flow calculation examples. Added filter for flow   |
| Example_Definitions.h                                     | Initial commit   |
| UFC23_Utils.cpp   | Initial commit   |
| UFC23_Utils.h   | Initial commit   |

Figure 28: GitHub example library (subject to changes)

## 11 Soldering information

The ENS160 uses an open LGA package. This package can be soldered using a standard reflow process in accordance with IPC/JEDEC J-STD-020D (Figure 29).

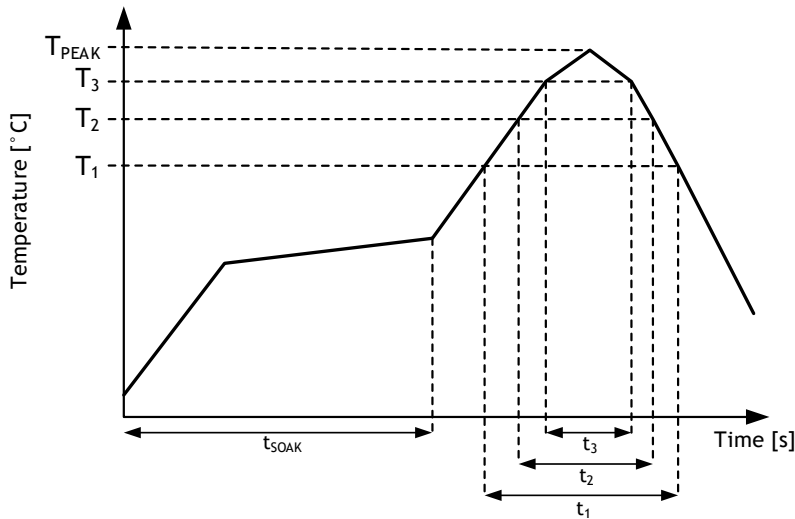


Figure 29: Solder reflow profile graph

The detailed settings for the reflow profile are shown in Table 63.

Table 63: Solder Reflow Profile

| Parameter                                  | Reference  | Rate / Unit |
|--|------------|-------------|
| Average temperature gradient in preheating |            | 2.5 K/s     |
| Soak time                                  | $t_{SOAK}$ | 2..3 min    |
| Soak temp range                            | Ts max     | 200°C       |
|  | Ts min     | 150°C       |
| Time above 217°C (T1)                      | $t_1$      | Max. 60s    |
| Time above 230°C (T2)                      | $t_2$      | Max. 50s    |
| Time above TPEAK -10°C (T3)                | $t_3$      | Max. 10s    |
| Peak temperature in reflow                 | $T_{PEAK}$ | 260°C       |
| Temperature gradient in cooling            |            | Max. -5K/s  |

It is recommended to use a no-clean solder paste. There should not be any board wash processes, to prevent cleaning agents or other liquid materials contacting the sensor area.

## 12 Package drawings & markings

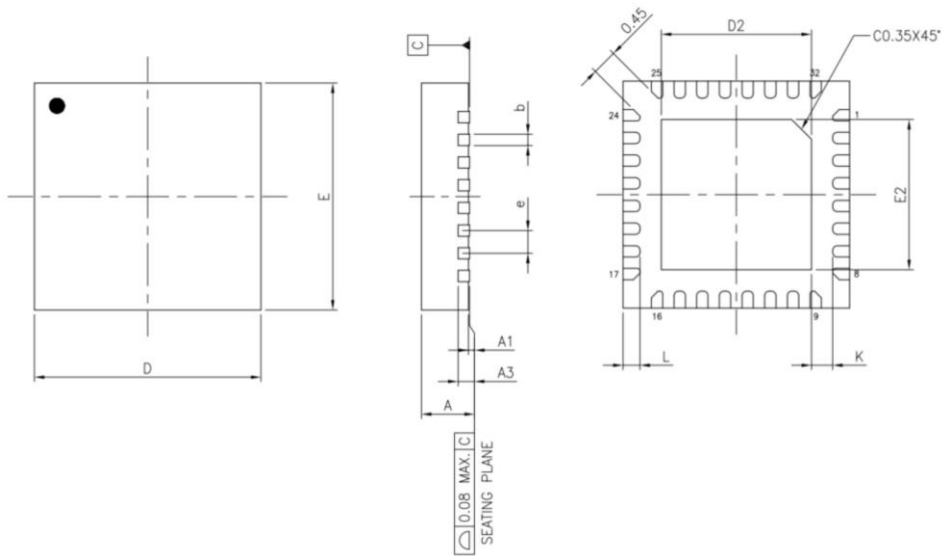


Figure 30: QFN32 package drawing

Table 64: QFN32 package dimensions

| Symbol                 | Dimensions |         |      |
|------------------------|------------|---------|------|
|                        | Min        | Nominal | Max  |
| A                      | 0.80       | 0.85    | 0.90 |
| A1                     | 0.00       | 0.02    | 0.05 |
| A3                     | 0.203 REF. |         |      |
| b                      | 0.15       | 0.20    | 0.25 |
| D, E                   | 3.90       | 4.00    | 4.10 |
| D2, E2                 | 2.40       | 2.50    | 2.60 |
| e                      | 0.40 BSC   |         |      |
| L                      | 0.35       | 0.40    | 0.45 |
| K                      | 0.20       | -       | -    |
| Pad size<br>118x11 MIL | 2.65       | 2.70    | 2.75 |

**Note(s):**

1. All dimensions are in millimeters.
2. PCB land pattern are shown as red dotted lines.
3. Add 0.05mm all around the nominal lead width and length for the PCB land pattern.

●  
**UFC23**  
**LQF**  
**YYWW**

YY = Year, WW = Week

Figure 31: QFN32 package marking

Tape & Reel

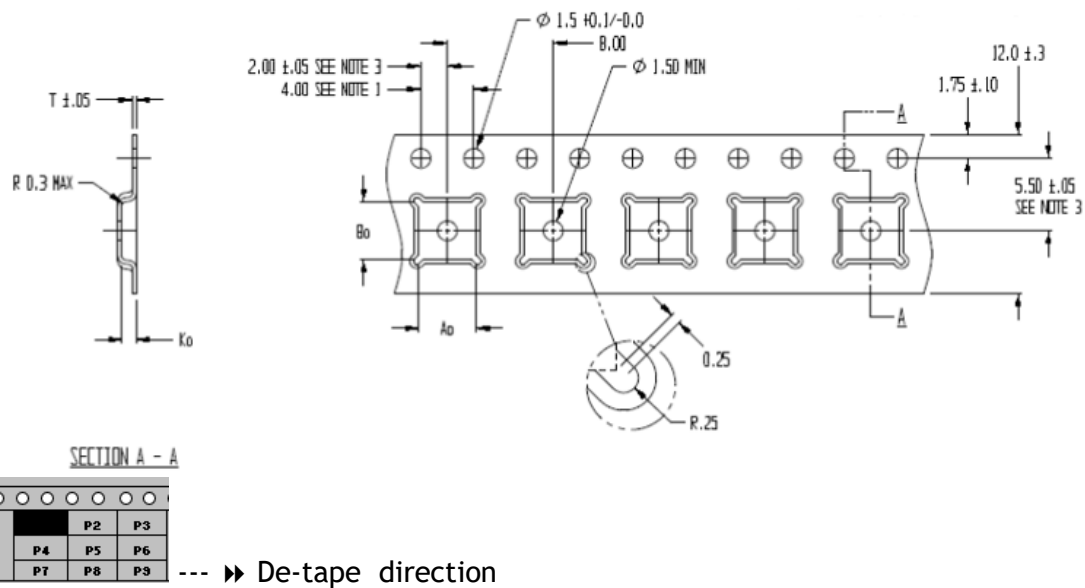


Figure 32: Tape drawing

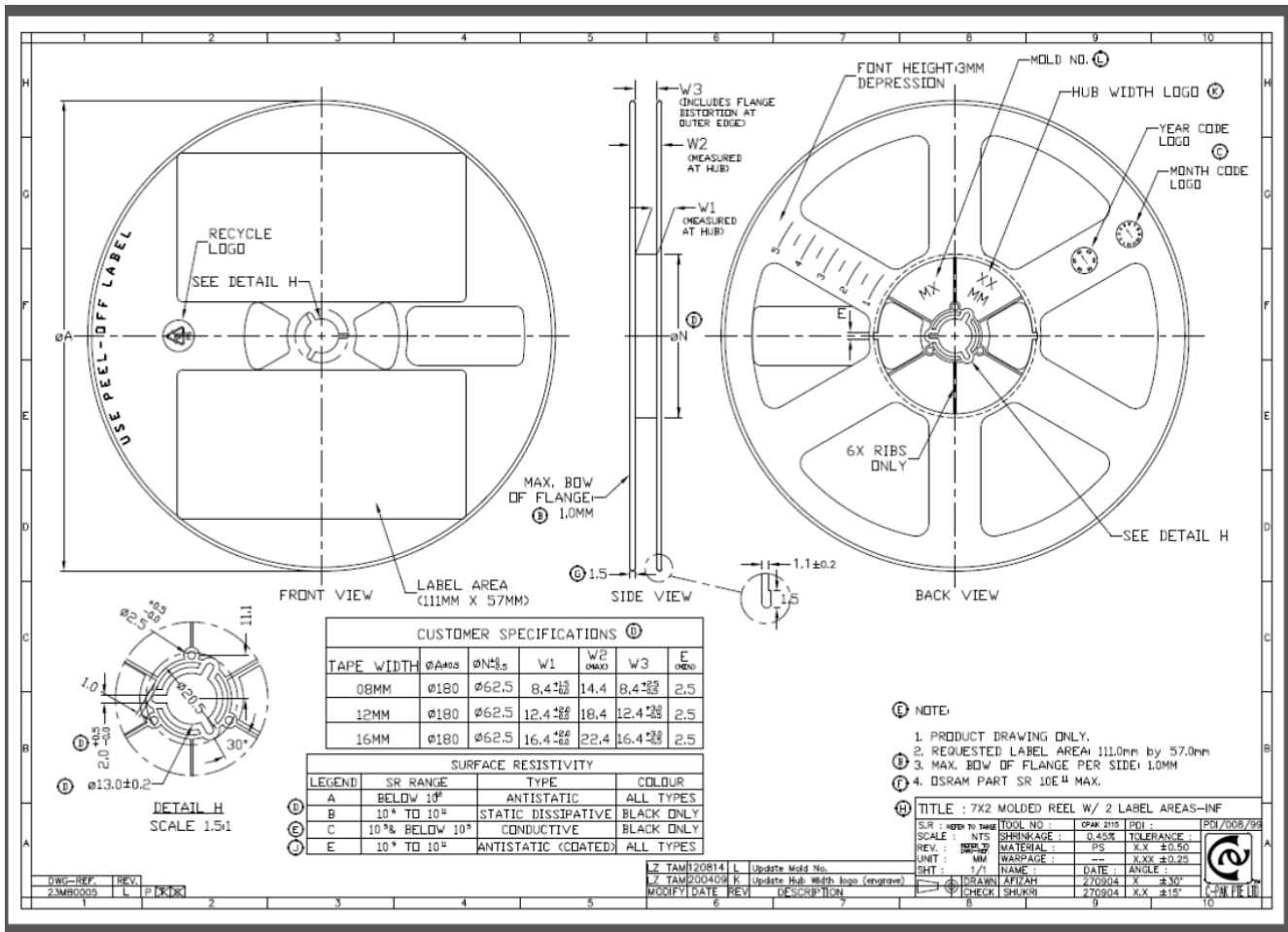


Figure 33: Reel drawing

### 13 Ordering information

Table 65: Ordering information

| Ordering Code | Material ID | Package | Delivery Form | Delivery Quantity |
|---------------|-------------|---------|---------------|-------------------|
| UFC23-LQFT    | 502090004   | QFN32   | Tape & reel   | 1000 pcs          |

## 14 RoHS Compliance & ScioSense Green Statement

**RoHS:** The term RoHS compliant means that Sciosense B.V. products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead does not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

**ScioSense Green (RoHS compliant and no Sb/Br):** ScioSense Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

**Important Information:** The information provided in this statement represents Sciosense B.V. knowledge and belief as of the date that it is provided. Sciosense B.V. bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. Sciosense B.V. has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. Sciosense B.V. and Sciosense B.V. suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

## 15 Copyrights & Disclaimer

Copyright Sciosense B.V High Tech Campus 10, 5656 AE Eindhoven, The Netherlands. Trademarks Registered. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

Devices sold by Sciosense B.V. are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. Sciosense B.V. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. Sciosense B.V. reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Sciosense B.V. for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Sciosense B.V. for each application. This product is provided by Sciosense B.V. "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

Sciosense B.V. shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Sciosense B.V. rendering of technical or other services.

## 16 Document status

Table 66: Document status

| Document Status          | Product Status  | Definition   |
|--------------------------|-----------------|--|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice.   |
| Preliminary Datasheet    | Pre-Production  | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice.                   |
| Datasheet                | Production      | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of SciSense B.V. standard warranty as given in the General Terms of Trade.                                |
| Datasheet (Discontinued) | Discontinued    | Information in this datasheet is based on products which conform to specifications in accordance with the terms of SciSense B.V. standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs. |

## 17 Revision information

Table 67: Revision history

| Revision | Date       | Comment   | Page                                       |
|----------|------------|---|--|
| N        | 29.04.2026 | PGA drawings updated<br>RAM section updated<br>GitHub as code reference added | Section 6.4<br>Section 8.2<br>Section 10.2 |
| 1        | 07.05.2026 | First release for product launch  | All  |

### Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

**Address:** Sciosense B.V.  
High Tech Campus 10  
5656 AE Eindhoven  
The Netherlands

**Contact:** [www.sciosense.com](http://www.sciosense.com)  
[info@sciosense.com](mailto:info@sciosense.com)